Soft-switching capability analysis of a qZSI-based DC/DC converter

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ABSTRACT: This paper analyzes the PWM control method for a new type of step-up DC/DC converters with galvanic isolation - the quasi-Z-source inverter (qZSI) based DC/DC converter. The PWM control method for qZSI with soft-switching capability is proposed and experimentally proved. The operation principles of discussed converter are explained. The experimental verification and analysis of top and bottom IGBTs of inverter bridge has been made. A prototype has been built in the laboratory and experiments are presented to analyse the soft-switching capability in loss reduction.

1 Introduction

In 2009 researchers of the Department of Electrical Drives and Power Electronics of Tallinn University of Technoogy proposed the new qZSI-based step-up DC/DC isolated converter [1], [2]. The simplified power circuit layout is presented in Fig. 1.

The converter consists of:

- the quasi-Z-source network (qZS-network) that includes two capacitors (*C1* and *C2*), diode (*D1*) and coupled inductors (*L1* and *L2*);
- snubber circuit (*D4*, *D5*, *D6*, *C5*, *C6*, *C7*) for absorbing the transient overvoltages across the DC-link caused by stray inductances;
- IGBT based inverter (*T1* - *T4*);
- high-frequency step-up isolation transformer;
- voltage doubler rectifier (VDR) used in order to reduce the transformer turn ratio.

Since the proposed qZSI based DC/DC converter is intended for low voltage stepping up, high current values in the input side of the converter at high power ratings of the system are unavoidable. It means that serious attention should be paid to loss reduction not only in conductors [3] but also in semiconductor switches of inverter. The significant loss reduction in IGBT switches can be achieved by implementation of proper control method in order to reach soft switching.

2 Operation Principles of Converter

The desired DC-link voltage level of proposed converter could be selected in accordance with the characteristics of the voltage source implemented.

Based on the input voltage, the operating modes of the proposed DC/DC converter could be broadly categorized as non-shoot-through and shoot-through operating modes (Fig. 2) [4].

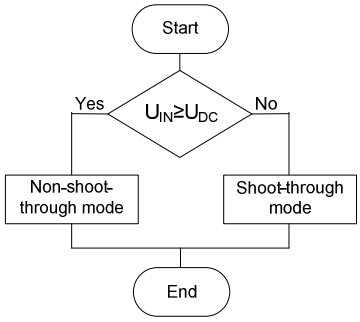

Fig. 2. Flow chart of operating modes of qZSI based DC/DC converter [4]

If the input voltage is equal or higher than the desired DC-link voltage, the converter works in the non-shoot-through mode. In this mode, the qZSI operates as a traditional VSI performing only the buck function of the input voltage. The operating period of the qZSI in the non-shoot-through operating mode consists of the combination of active and zero states and is explained in more detail in [4].

If the input voltage drops below the predefined DC-link voltage level, the converter starts to operate in the shoot-through mode. During the shoot-through states the primary winding of the isolation transformer is shorted through both the upper and lower switches of any one phase leg (i.e., both devices are gated on) or all two phase legs [4].

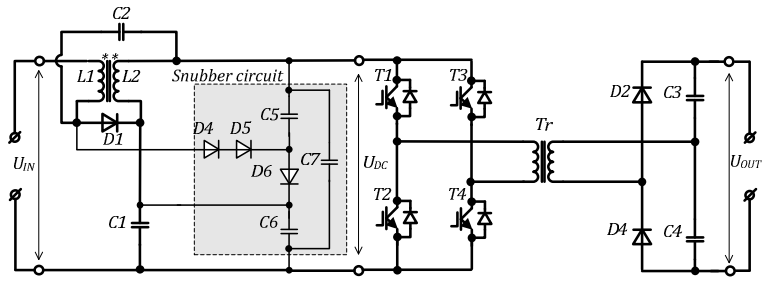

Fig.1. Simplified power circuit diagram of the proposed converter

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3 Shoot-Through Control Method

A new pulse width modulation (PWM) shoot-through control method for the qZSI based DC/DC converter is used [4]. Shoot-through is generated during zero states. The zero and shoot-through states are spread over the switching period so that the number of higher harmonics in the transformer primary could be reduced. In order to reduce switching losses of the transistors, the number of shoot-through states per period was limited by two. Moreover, in order to decrease the conduction losses of the transistors, the shoot-through current is distributed between both inverter legs.

In the proposed control method an operating period consists of three states: active, zero and shoot-through state (Fig. 3). Active state means that only one switch in each phase leg conducts. In the zero state the primary winding of the isolation transformer is shorted through either the top- (*T1* and *T3*) or bottom-side (*T2* and *T4*) inverter switches. Shoot-through states (all transistors conducting) are created during the zero states of the full-bridge inverter. To provide a sufficient regulation margin, the zero state time t_Z should always exceed the maximum duration of the shoot-through states per one switching period. In general, each operating period of the qZSI during the shoot-through mode always consists of an active state t_A, shoot-through state t_S and zero state t_Z:

$$T = t_A + t_S + t_Z. \tag{1}$$

Eq. (1) could be also represented as

$$\frac{t_A}{T} + \frac{t_S}{T} + \frac{t_Z}{T} = D_A + D_S + D_Z = 1, \tag{2}$$

where D_A is the duty cycle of an active state, D_S is the duty cycle of a shoot-through state and D_Z is the duty cycle of a zero state.

The converter was studied at the minimal allowable input voltage when maximal voltage boost is demanded. It means that this is the heaviest working point for transistors because of the highest currents in the converter input side elements and the inverter bridge. In this mode the gating signals are set with the following parameters: maximal shoot-through D_S=0.25, duty cycle of active states D_A=0.5 and duty cycle of zero states D_Z=0.25.

Fig. 3 shows the gating signal diagram of proposed control method. Zero states in the case of PWM are always generated by the same switches either the top (*T1* and *T3*) or the bottom (*T2* and *T4*) inverter switches. Two shoot-through states are generated. During this operating mode the current through inverter switches reaches its maximum. The voltage across the inverter bridge (U_{DC}) drops to zero and the resulting primary winding voltage waveform (U_{Tr}) of the isolation transformer is indicated in Fig. 3.

Regarding to this methodology the switching states sequence is shown in Table I.

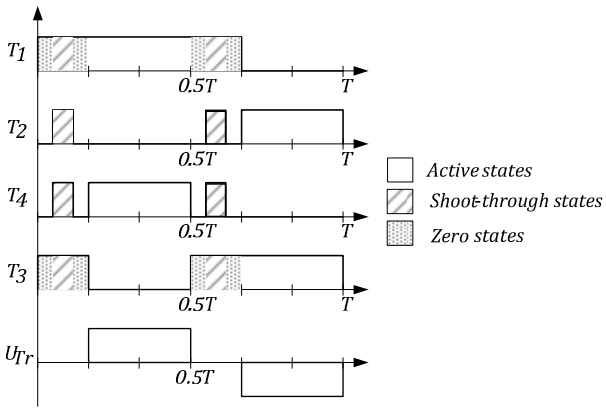

Fig. 3. Generation of PWM signals with shoot-through during zero states.

The states are shown for one switching period of the isolation transformer. As it can be seen, the transistors work with different number of commutations per period, thus they have unequal switching losses. Top transistors *T1* and *T3* have two commutations per period while bottom transistors *T2* and *T4* have three times more commutations per period.

TABLE I
PWM SWITCHING STATES SEQUENCE PER ONE PERIOD

	T1	T2	T3	T4
zero state	1	0	1	0
shoot-through	1	1	1	1
zero state	1	0	1	0
active state	1	0	0	1
zero state	1	0	1	0
shoot-through	1	1	1	1
zero state	1	0	1	0
active state	0	1	1	0

4 Experimental Verification

To verify the presented theoretical assumptions an experimental setup of the qZSI-based single-phase DC/DC converter was developed and tested. Operating parameters of the investigated converter in Table II were selected for the case of maximal voltage boost when maximal current in the input side of converter appear.

TABLE II
GENERAL PARAMETERS OF THE INVESTIGATED CONVERTER

Parameter	Value
Input voltage, U_{IN}	40 V
Desired DC-link voltage, U_{DC}	80 V
System power rating	840 W
Operation frequency of qZS-network, f_{qZS}	10000 Hz
Operation frequency of isolation transformer, f_{Tr}	5000 Hz
Shoot-through duty cycle, D_S	0.25
Active state duty cycle, D_A	0.5
Type of IGBTs	IXGH 32N60BU1

Since the operation of top (*T1* and *T3*) and bottom (*T2*, *T4*) transistors is different, each group will be discussed separately. Moreover, both qZSI legs are operating

identically, that is why measurements were made on one leg transistors *T1* (top) and *T2* (bottom).

Collector emitter voltage U_{CE} and collector current I_C switching transients were measured with digital oscilloscope *Tektronix TPS2024*, differential voltage probe *Tektronix P5205* and current probe LEM HEME PR 30. Measured data were acquired in tabular form and later processed in MS Exel. Using acquired data IGBT losses were calculated by help of Eqs. (3)...(7).

The turn-on losses of transistor can be calculated as

$$P_{ON} = f \cdot \int_{t_1}^{t_2} I_C \cdot U_{CE} \cdot dt, \tag{3}$$

where f is operating frequency, t_1 is the limit of 10% I_C rise and t_2 is the limit of 90% U_{CE} fall [5].

The turn-off losses of transistor can be found as

$$P_{OFF} = f \cdot \int_{t_3}^{t_4} I_C \cdot U_{CE} \cdot dt, \tag{4}$$

where t_3 is the limit of 10% U_{CE} rise and t_4 is the limit of 90% I_C fall [5].

The total dynamic losses in transistor can be calculated as

$$P_{Dyn} = P_{ON} + P_{OFF}. \tag{5}$$

Static losses in transistor can be found as

$$P_{Stat} = f \cdot \int_{t_2}^{t_3} U_{CE} \cdot I_C \cdot dt. \tag{6}$$

The total losses in transistor can be found as

$$P_{TOTAL} = P_{Dyn} + P_{Stat} \tag{7}$$

4.1 Operation Conditions of Top Switches

Fig. 4 shows the experimental waveforms of transistor *T1* collector emitter voltage U_{CE}, collector current I_C and power loss P_{Loss}. It can be seen that the waveforms in both shoot-through states (S1 and S2) are identical in terms of voltage (U_{CE}) and current (I_C), thus in the further discussion only one shoot-through state is analyzed. All the turn-on/off and conduction intervals are outlined with dashed lines.

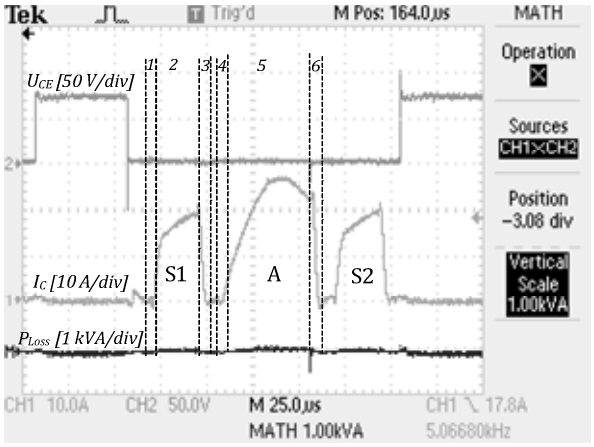

Fig. 4. Experimental waveforms of one switching period of top transistors

Generally, it can be seen that because of the inherent properties of scheme control algorithm the top transistor is soft-switched in whole period, but for to be sure about that, the detailed examination of turn-on/off intervals will be made.

Figs. 5*a* and 5*b* show the turn-on and turn-off intervals (1 and 3) of the shoot-through state according to Fig. 4. It is obvious that shoot-through states are soft-switched.

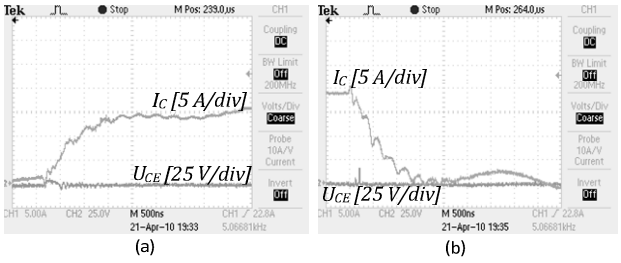

Fig. 5. Shoot-through state turn-on (a) and turn-off (b) intervals of top transistors

Figs. 6*a* and 6*b* show the turn-on and turn-off intervals (4 and 6) of the active state according to Fig. 4. It is seen that during both intervals the IGBT is soft switched.

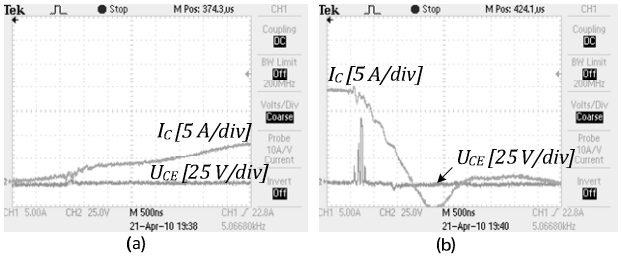

Fig. 6. Active state turn-on (a) and turn-off (b) intervals of top transistors

Comparison between the static and dynamic losses for one top transistor for one operating period is summarized in Table III. It can conclude that static losses comprise 94% of whole losses in one transistor. In addition, the Table III shows that static losses in active state and in both shoot-through states are almost equal.

TABLE III

COMPARISON OF TOP TRANSISTOR LOSSES

State \ Losses	P_{ON} (W)	P_{OFF} (W)	P_{Stat} (W)
Shoot-through	0.28	0.5	10
Active	0.014	0.57	11.67

4.2 Operation Conditions of Bottom Switches

Fig. 7 shows the transistor *T2* collector emitter voltage U_{CE}, collector current I_C and power loss P_{Loss} experimental waveforms. It can be seen that the waveform in both shoot-through states (S1 and S2) are identical in terms of voltage (U_{CE}) and current (I_C), thus in the further discussion only one shoot-through state is analyzed. All the turn-on, turn-off and conduction intervals are outlined with dashed lines. Power loss P_{Loss} waveform already shows that shoot-through and active state turn-off (intervals 3 and 6) are hard-switched.

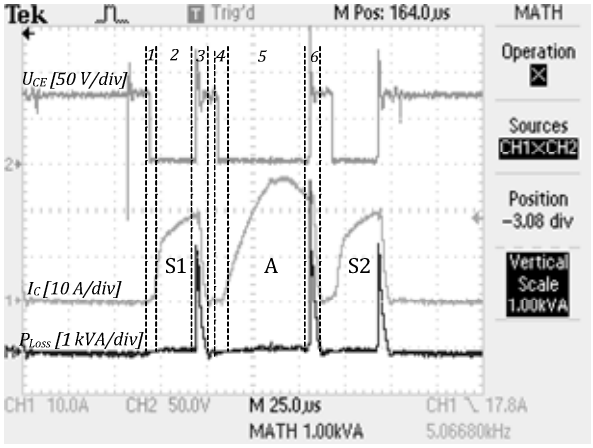

Fig. 7. Experimental waveforms of one switching period of bottom transistors

Figs. 8*a* and 8*b* show the turn-on and turn-off intervals (1 and 3) of the shoot-through state according to Fig. 7. It is seen that during turn-on of the shoot-through state the transistor is soft switched (Fig. 8*a*), but during turn-off of the shoot-through state the transistor is hard-switched (Fig. 8*b*).

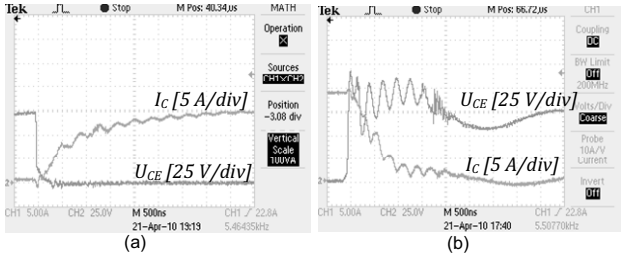

Fig. 8. Shoot-through state turn-on (a) and turn-off (b) intervals of bottom transistors

Figs. 9*a* and 9*b* show the turn-on and turn-off intervals (4 and 6) of the active state according to Fig. 7. It is seen that during turn-on of the active state the transistor is soft switched (Fig. 9*a*), but during turn-off of the active state the transistor is hard-switched (Fig. 9*b*).

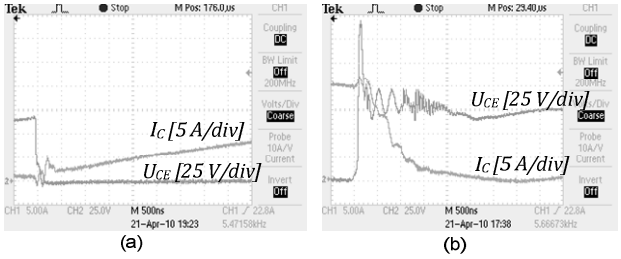

Fig. 9. Active state turn-on (a) and turn-off (b) intervals of bottom transistors

Comparison between the bottom transistor losses is given in Table IV.

TABLE IV

COMPARISON OF BOTTOM TRANSISTOR LOSSES

Losses / State	P_{ON} (W)	P_{OFF} (W)	P_{Stat} (W)
Shoot through	0.55	18.6	13.5
Active	0.35	5.1	9.4

It is obvious that the most significant part of dynamic losses is comprised by hard-switched turn-off losses (96%). Table V shows that static and dynamic losses in bottom transistor are almost the same.

5 Conclusions and Future Work

This paper presents the shoot-through PWM control method for the qZSI based DC/DC converter. First, the qZSI based DC/DC converter topology was described in general terms. Then, operating principles of the PWM modulation method were explained with the help of the switching diagram and state table.

The practical part of paper is focussed on the analysis of power losses in inverter bridge. Due to implemented control algorithm, the top group IGBTs of inverter bridge are soft-switched while bottom group IGBTs are hard-switched. This fact reflects in the top and bottom IGBT power losses that are shown in Table V. As Table V presents, conduction losses in both transistor groups are almost equal while dynamic losses in the top group make up only 5% of the whole dynamic losses in the qZSI. This fact reflects in total power loss balance.

TABLE V

COMPARISON OF INVERTER LOSSES

Losses / Group	P_{Dyn} (W)	P_{Stat} (W)	P_{TOTAL} (W)
Top group	2.7	43.3	46
Bottom group	49.2	45.8	95

In the further research, the optimization of control algorithm will be in order to increase the soft-switching capabilities of qZSI-based DC/DC converter and to further reduce the dynamic losses.

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