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Practical Design Guidelines of qZSI Based Step-Up DC/DC Converter

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Abstract. **This paper presents some design guidelines for a new voltage fed step-up DC/DC isolated converter. The most significant advantage of proposed converter is voltage buck-boost operation on single stage. The most promising application for proposed converter is in the field of distributed power generation e.g. fuel cells or photovoltaic.**

The most sensitive issues - such as power losses caused by high currents in the input side of converter and high transient overvoltages across the inverter bridge caused by stray inductances were discussed and solved. The proposals and recommendations to overcome these issues are given in the paper. The Selection and design guidelines of converter elements are proposed and explained.

The prototype of proposed converter was built and experimentally tested. Some results are presented and evaluated.

Keywords: **DC/DC power conversion, impedance converters**

I. INTRODUCTION

The paper presents a brand new step up DC/DC converter topology for distributed power generation (Fig. 1). Detailed design guidelines and analysis of proposed voltage-fed quasi-Z-source inverter based isolated DC/DC step-up converter was presented by authors in [1].

The main distinction and major advantage of the proposed converter is voltage buck-boost operation in a single stage that results in lower costs and decreased losses. The difference between the proposed converter and the conventional voltage stepping-up converter is in the use of the unique connection of coupled inductor (*L1* and *L2*), two capacitors (*C1* and *C2*) and the diode (*D1*), called quasi-Z-source (qZS) network [2], [3]. The qZS-network allows utilizing an extra switching state of converter called – shoot-through state. The shoot through state is simultaneous conduction of both switches in the same phase leg of inverter. The shoot-through state is forbidden in the traditional VSI, because it will cause a short circuit of the voltage source and damage the devices. One more distinction of the proposed converter is that it always has continuous input current during the shoot-through operating mode.

This paper covers hardware optimization methods and practical design guidelines in order to increase converter efficiency, because the proposed converter is a step-up converter, i.e. it has minimal voltage and maximal current on the input side, but maximal voltage and minimal current on the output. Therefore, to achieve better performance special attention should be paid to the design of the converter.

The converter was studied at the minimal allowable input voltage when maximal voltage boost is demanded. It means that this is the heaviest working point for transistors because of the highest currents in the converter input side elements and the inverter bridge.

To improve converter efficiency the following considerations should be taken into account:

- loss minimization on the input side of the converter. Since stepping-up of low voltage is always connected with high currents on the converter input side (qZS-network), passive elements (capacitors and coupled inductors), semiconductors and wiring techniques should be selected properly in order to reduce active power losses and increase converter efficiency and reliability. Moreover, improved converter efficiency enables dimensions to be reduced, which would raise power density;
- loss minimization in converter semiconductor elements. Losses in semiconductor bridge transistors mostly depend on the operation current. To minimize losses it is necessary to select transistors with better characteristics and choose a control algorithm;
- special attention should be paid to operating voltages of the qZS-network diode and the inverter bridge. The specific and problematic issue of a converter is voltage overshoots on the qZS-network diode and the inverter bridge caused by stray inductance. These phenomena can destroy semiconductor switches or cause the undesired power dissipation and EMI. To cope with those problems snubber circuits should be studied.

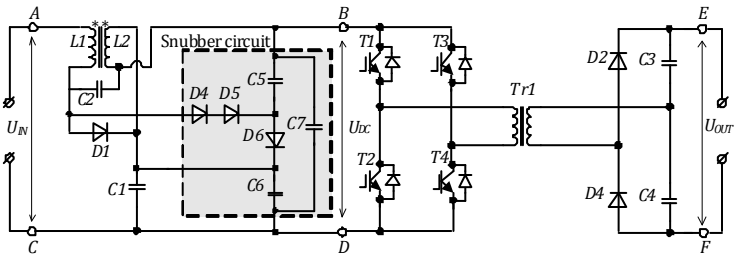


Fig. 1. Simplified power circuit diagram of the proposed converter.

Operating parameters of the investigated converter are presented in Table I.

TABLE I
GENERAL PARAMETERS OF THE PROPOSED SYSTEM

Parameter	Value
Input voltage U_{IN}	40 V
Desired DC-link voltage U_{DC}	80 V
DC- load R	400 Ω
Isolating transformer ratio n	1:3.75
qZS-network operation frequency f_{qZS}	10000 Hz
Transformer operation frequency f_{T1}	5000 Hz
Inductor current ripple r_C	25%
Shoot-through duty cycle D_S	0.25

II. LOSS MINIMIZATION ON THE INPUT SIDE OF THE CONVERTER

Since the qZS inverter (qZSI) based boost converter is intended for low voltage (40 V) stepping up (600 V), high current values in the qZS-network at high power ratings of the system are unavoidable. High currents occur especially during shoot-through states. Since losses (I^2R) are directly proportional to the current, serious attention should be paid to conductor design and selection.

A. Loss Minimization in Conductors

If the power rating of our converter is, for example, 1000 W and the input voltage is 40 V, then the current at the converter input is 25 A. Power losses in the conductors are

$$P_{cond.losses} = I^2 R \ , \tag{1}$$

where

$$R = \rho \frac{l}{S} \ , \tag{2}$$

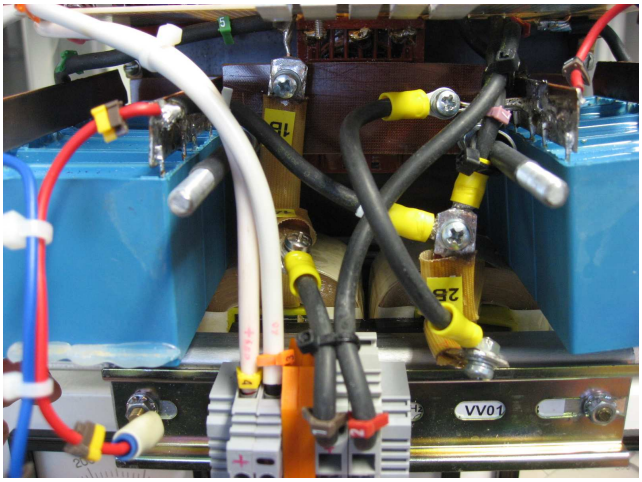
where ρ is the resistivity of the conductor, l is the length of the conductor and S is the cross-sectional area of current flow. It is obvious from (2) that active resistance of the wire can be reduced using wires with a large cross-sectional area. Additional resistance of a conductor can cause cable sleeves, screws and their connection points. The connection image and thermo image of the qZS-network is shown in Fig. 2*a* and 2*b*.

The thermo image (Fig. 2*b*) shows an approximate temperature of qZS-network connecting wires (circled around with oval lines), i.e. $T \approx 42$°C.

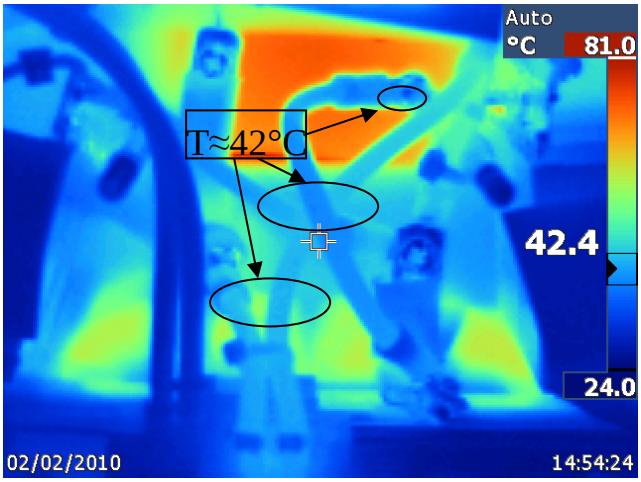
To minimize the undesired power dissipation it can be recommended that in the place of wire and cable sleeves printed circuit boards (PCB) (for low power conversion) or laminated copper busbars (for high power conversion) are highly recommended to be implemented [4], [5]. The nominal current for PCBs trace can be found as

$$I = k \cdot \Delta T^{0.44} \cdot n \cdot A^{0.725}, \tag{3}$$

where I is maximum current (A), ΔT is temperature rise above



(a)



(b)

Fig. 2. Conductors of the qZS network (a) and thermo image (b) qZS-network.

ambient (°*C*), *A* is cross-sectional area (m^2), *n* is conversion coefficient from square meter to square mils (n=1550003100), k=0.024 is used for inner layers and k=0.048 is used for outer (top or bottom) layers [6], [7].

Laminated copper busbars can be implemented not only to depress conduction losses but also to build capacitance, which could work as an additional input filter.

B. Loss Minimization in Semiconductors

Since the power semiconductors are situated on the primary side of the converter, high currents pass through the diode *D1* and inverter switches *T1-T4* can cause significant power losses. It means that very serious attention should be paid to loss estimation and selection of power semiconductors.

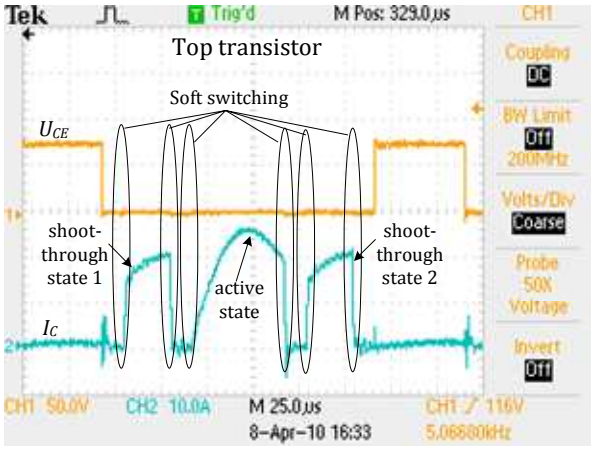
1. Loss minimization in transistors

In the PWM inverter, each switching device has to be selected according to the maximum voltage applied, the peak and average current going through it and operation frequency.

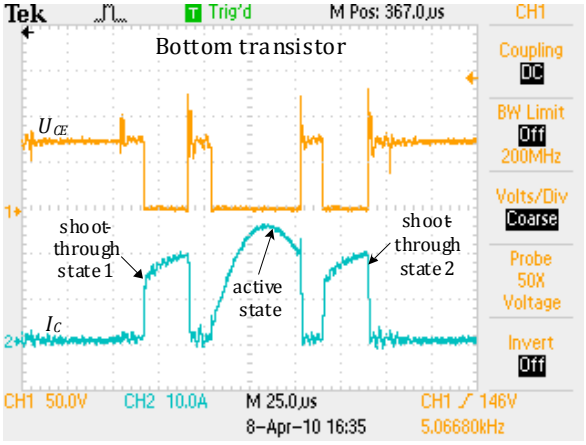
The hyper-fast IGBT transistor with low voltage drop (IXGH 32N60BU1) was selected in converter prototype. The oscillograms with voltage and current waveforms of the top

and bottom transistor of one inverter leg are shown in Fig. 3*a* and 3*b*, respectively.

Because of the successful control algorithm, the top transistors (*T1* and *T3*) are soft switched (Fig. 3*a*), but the bottom transistors (*T2* and *T4*) are hard switched (Fig. 3*b*).



(a)



(b)

Fig. 3. Voltage and current waveforms of transistors in one inverter leg: transistor *T1* – (a) and transistor *T2* – (b).

For estimation of static power losses, it is necessary to know saturation voltage U_{CE} from device datasheet determined by the function $U_{CE}=f(I_C)$.

As Fig. 3 shows, the current shape during both shoot-through states and the active state. Since the current shape is the same, the static losses are equal and can be estimated as

$$P_{stat} = I_{C(av)} \cdot U_{CE(sat)}, \tag{4}$$

where $I_{C(av)}$ is collector current, which for the shoot-through state can be calculated as

$$I_{C(av),S} = \frac{P \cdot D_S}{U_{IN}}, \tag{5}$$

where P is system power rating, U_{IN} is input voltage and D_S is shoot-through duty cycle.

For active state average collector current can be calculated as

$$I_{C(av),A} = \frac{P}{2 \cdot U_{DC}}, \tag{6}$$

where U_{DC} is DC-link voltage.

In the case of bottom transistors, dynamic losses should also be considered. The bottom transistor dynamic losses consist of two shoot-through state on/off switching losses active state on/off switching losses.

For estimation of dynamic losses (switching on/off losses), it is necessary to know other datasheet parameters: turn on energy dissipation E_{on}, determined by graphs $E_{on}=f(I_C)$; turn-off energy dissipation E_{off} determined by the graphs: $E_{off}=f(I_C)$. Dynamic losses can be calculated as

$$P_{dynamic} = (E_{on} + E_{off}) \cdot f, \tag{7}$$

where f is switching frequency.

Data sheet values of transistors dependent on I_C are presented in Table II.

TABLE II

TRANSISTOR PROPERTIES AT COLLECTOR CURRENT

State	I_C, A	$U_{CE(sat)}$, V	E_{on}, mJ	E_{off}, mJ
active state	12.5	1.4	0.37	0.38
shoot-through state	12.5	1.4	0.37	0.38

Taking into consideration those values, the resulting power losses of transistors are presented in Table III in comparison with experimentally measured values.

TABLE III

COMPARISON OF CALCULATED AND MESURED TRANSISTOR LOSSES

Loss	Top (calculated)	Top (measured)	Bottom (calculated)	Bottom (measured)
Static	17.5 W	18.5 W	17.5 W	18.7 W
Dynamic	0 W	0.9 W	11.2 W	15.4 W
Total	17.5 W	19.4 W	28.7 W	34.1 W

Because of soft switching of transistors *T1* and *T3* it can be concluded that dynamic losses are 0. The difference between the measured and calculated values could be because of the displacement of data sheet values and real values.

Since the conduction losses comprise the biggest part of losses, the switches with smaller forward voltage drop should be recommended.

2. Loss minimization in the diode

Since the Shottky diode is used, reverse-recovery losses can be neglected because the reverse-recovery time is very short. Consequently, the static losses of the diode are essential and can be calculated as

$$P_{stat} = I_F \cdot U_F, \tag{8}$$

where I_F is the average diode current, U_F is diode forward voltage drop during I_F. In proposed converter high voltage power Schottky rectifier (STPS160H100TV) was used. For

the implemented diode at I_F=25 A the U_F=0.275 V and static losses (P_{stat}) are 6.87 W.

III. Design Gudelines for the qZS-Network

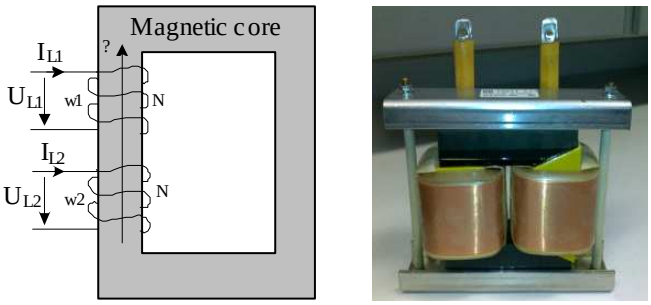
A. Coupled Inductor Design

In discussed qZS-network the shoot-through mode is used to boost the magnetic energy stored in the DC side inductors without short-circuiting DC capacitors. This increase in inductive energy in turn provides the boost of voltage seen on the transformer primary winding during the traditional operating states of the inverter. Respectively, coupled inductor provides necessary voltage boost in converter.

There are two possibilities for connecting inductor windings (*L1* and *L2*) – the common mode and the differential mode.
To minimize current ripple on the inductor, the windings should be connected in the differential mode [8], [9], but to minimize inductor size and weight, the windings should be connected in the common mode. Size and weight minimization can be explained as in [10], [11], [12]. For a single coil (Fig. 4) on one core, the flux through the core is

$$\phi = E \cdot N \cdot I_L, \tag{9}$$

where E is a constant related to the core material and dimensions, N is the number of turns of the coil and I_L is the average current through the coil.



(a) (b)

Fig. 4. Coupled inductor: principle (a) and 1.5 kW example (b).

The inductance of the coil is

$$L = \frac{N \cdot \phi}{I_L} = E \cdot N^2, \tag{10}$$

In the voltage-fed qZSI the currents through inductors *L1* and *L2* are always exactly the same (I_{L1}=I_{L2}=I_L) in terms of waveform and magnitude. For two coils on one core with exactly the same current, I_L, the flux through the core is

$$\phi = 2 \cdot E \cdot N \cdot I_L. \tag{11}$$

The resulting inductance of each winding when supplying exactly the same current to the two windings is

$$L = \frac{N \cdot \phi}{I_L} = 2 \cdot E \cdot N^2. \tag{12}$$

It is seen from (12) that the inductance of each winding is doubled. Therefore, for the same operating conditions we need to build two windings with twice-smaller inductance than in the case of separate inductors.

The inductor in the qZS-network will limit the current ripple through the switches during the shoot-through states. Operating voltage U_L and operating current I_L of one inductor winding *L1* are presented in Fig. 5 The inductor during the shoot-through state t_S stores the energy but during the active state t_A charges-up the capacitor *C1* with stored energy.
Inductance L of inductor *L1* can be expressed with (13)

$$L = \frac{U_L \cdot t_S}{\Delta i_L}, \tag{13}$$

where U_L is the inductor voltage, t_S is the shoot-through time and Δi_L is current changes in the inductor during t_S.

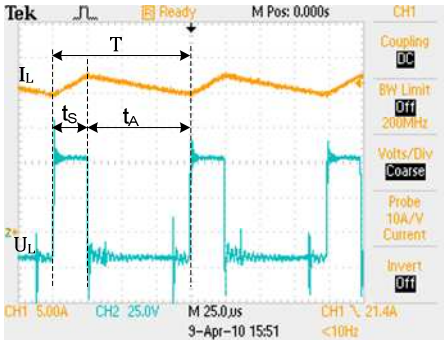


Fig. 5. Current and voltage waveforms in one winding.

A distinction of this scheme is that the inductor voltage during the shoot-through state is equal to capacitor *C1* voltage U_{C1} [1]

$$U_L = U_{C1} = U_{IN} \frac{1 - \frac{t_S}{T}}{1 - 2 \cdot \frac{t_S}{T}}. \tag{14}$$

Taking into account the above and choosing an acceptable peak to peak current ripple r_C, the inductance (13) can be transformed as

$$L = \frac{U_L \cdot t_S}{\Delta i_L} = \frac{U_{C1} \cdot t_S}{I_L \cdot r_C} = \frac{U_{IN} \frac{1 - \frac{t_S}{T}}{1 - 2 \cdot \frac{t_S}{T}} \cdot t_S}{\frac{P}{U_{IN}} \cdot r_C}, \tag{15}$$

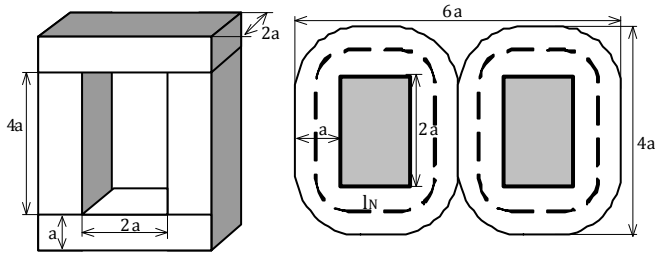
where P is the power rating of the converter, U_{IN} is the input voltage, r_C is the desired peak to peak current ripple through the inductor *L1* ($I_{p\text{-}p}/I_{av}$).

This section describes design guidelines of the coupled inductor. The basic calculation method can be used as suggested in [13]. Parameters for the calculations are presented in Table IV.

TABLE IV
ASSUMPTIONS FOR INDUCTOR CALCULATION

Parameter	Value
Current density in wire j	2·106 A/m^2
Saturation induction B_m	0.3 T
Window utilization factor k_a	0.35
Demanded inductance L	0.8 mH

Also, an assumed optimal geometry of the inductor is presented there (Fig.6).



(a) (b)

Fig. 6. Assumed inductor geometry: isometric view (a), lateral section (b).

The number of turns (N) can be calculated as

$$N = \frac{I_L \cdot L}{B_m \cdot S}, \tag{16}$$

where the cross-sectional area S of the inductor core can be calculated as

$$S_{core} = 2a^2. \tag{17}$$

The number of turns in coupled inductor (in both coils) can be calculated as

$$N = \frac{8 \cdot a^2 \cdot k_a \cdot j}{I_L}. \tag{18}$$

Inserting (17) and (18) in (16) we obtain the width of the core sheet

$$a = \sqrt[4]{\frac{L \cdot I_L^2}{16 \cdot N \cdot k_a \cdot j \cdot B_m}}. \tag{19}$$

The active resistance of one winding is

$$R_N = \rho_w \cdot \frac{l_N \cdot N \cdot j}{2I_L}, \tag{20}$$

where ρ_w=0,02.10^{-6} (Ω·m) is the approximate resistivity of copper wire, l_N is the average length of one turn in the winding (l_N=10a).
Power losses in one winding can be found as

$$\Delta P_N = I_L^2 \cdot R_N. \tag{21}$$

Specific surface losses can be obtained

$$q = \frac{\Delta P_1}{S_{cool}}, \tag{22}$$

where S_{cool} is the cooling area of the winding. Regarding to accepted geometry of inductor S_{cool}=56a^2, where the rectangle edge of the winding with high 4a and perimeter 14a is assumed as the cooling surface.
Heat can be evaluated from (22). Specific surface losses q should be $1100 \le q \le 1200$ (W/m^2).
If q is smaller than the given margins, then the current density j in the conductor can be increased. Diameter of the conductor is

$$d_{cond} = \frac{I_L}{j}. \tag{23}$$

Based on the equations previously described, the results are summarized in Table V.

TABLE V
SPECIFICATIONS OF THE DEVELOPED INDUCTOR

Parameter	Value
Number of turns in one winding N	43 turns
Core cross-sectional area S_{core}	7.7·10-4 m^2
Active resistance of one winding R_N	0.014 Ω
Power losses in one winding ΔP_N	8.5 W
Specific surface losses q	392 W/m^2
Conductor diameter d_{cond}	1.2·10-5 m^2

B. Power losses in the inductor

Power losses in the inductor come from core losses and copper losses. Core losses include hysteresis loss and eddy current loss in the magnetic cores. Copper losses are due to the skin effect and proximity effect, which will increase the equivalent ac resistance, R_{AC}, of magnetic wires or I^2R loss, where R=R_{AC}+R_{DC} [14], [15].

To reduce any temperature rise, either core loss by lowering the flux density and/or switching frequency can be reduced, as shown in the following equation [16]:

$$P_{Hysteresis} = k \cdot f^{\alpha} \cdot (B_{AC})^{\beta}, \tag{24}$$

where $P_{Hysteresis}$ is the hysteresis loss of ferrite materials (W/m^3), k, core constant, α is frequency constant and β is flux density constant, f is the switching frequency of the inductor and B_{AC} is AC flux density. Fig.7 shows our selected coupled inductor's ("Epcos" core material N27) relative core losses versus frequency at B_{max}=0.3 T and T=25 °C.

Soft ferrites have the highest resistivity among other materials and the eddy current loss is thus usually not a serious issue [16]. This makes it prominent in high switching frequency applications.

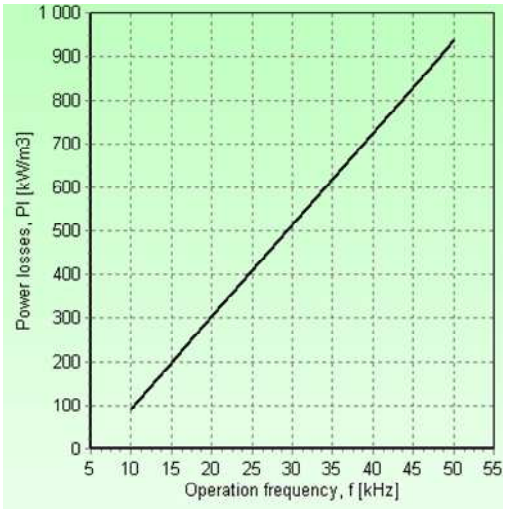


Fig. 7. Inductor relative core (material type N27) losses versus operation frequency.

Use of stranded wires, foil or Litz wires is a practical solution to minimize copper losses, and decreasing the switching frequency can also relieve the skin effect. In the proposed inductor the foil conductor is used because it is possible to wound the winding more compressed and the foil is much cheaper than Litz wire.

C. Selection of Magnetic Core

Many different core sizes and shapes are available in the market for different applications. The most suitable magnetic core for the coupled inductor in high power applications are the UI and E types [16]. They are low cost as compared with other core shapes and because of the simple bobbin structure which has a wide window it is easy to make a winding. Furthermore, a variety of sizes are available for choice to suite almost any application. All of these features make it the most popular core used in power circuits.

D. Selection of Capacitors

The main purpose of capacitors (*C1* and *C2*) in the qZS-network is to absorb the current ripple and limit the voltage ripple across the inverter bridge [17]. Caused by transient processes, the high voltage overshoots could occur on the qZS-network capacitors (Fig. 8*a*). To increase reliability and operation flexibility the polymer film capacitors can be recommended for capacitors of the qZS-network (*C1* and *C2*). The performance advantages of polymer film capacitors are electrical stability under AC and DC voltages, electrical and physical stability over temperature, resilience under thermal shock, stability under mechanical stress, ultra-low ESR, dissipation factor lower than 1% and high voltage capability up to 500 V_{DC}. As a result of comparison of all these properties, prices and manufacturer suggestions polypropylene film capacitors (Epcos B32778, 800 V, 60 μF) were selected for our converter prototype.

E. Selection of Diode

Diode *D1* is one of the most important elements in qZS-network. During the active state, it is forward biased, but during the shoot-through state, it is reverse-biased and does not allow to shorten the voltage source.

During the diode selection, special attention should be paid to the switching properties of it, i.e. the fast recovery diodes should be preferred to ensure proper recovery times. The forward voltage drop U_F is another important issue, because the high values of U_F could cause high conduction losses during active states, which, in turn, could seriously affect the efficiency of the converter.

IV. Snubber Circuit

Special attention should be paid to operating voltages and currents of the diodes and transistors. In real practice due to stray inductances and capacitances, very high transient overvoltages and parasitic ringings can occur. Finally, it could destroy the diode and transistors or cause the undesired power dissipation and EMI. To cope with those problems the snubber circuits should be implemented.

The basic structure for the snubber circuit was taken from [10]. Two capacitors *C5* and *C6*, and diode *D6*, all connected in series, as shown in Fig. 8, are connected in parallel to the inverter bridge. The other two diodes, *D4* and *D5*, in series are connected to the main power circuit from the snubber circuit forming a discharge loop for *C5*. Capacitor *C7* was put in parallel with the inverter bridge and along with capacitor *C5* and *C6*, and diode *D6* series connection.

Snubber circuit operation can be explained in two steps – absorbing of overvoltage peaks (charging of snubber capacitors *C5*, *C6* and *C7*) and discharging of snubber circuit capacitors. As seen from Fig. 8*a*, when the current to the inverter I_i has step changes, the DC rail snubber provides an extra absorbing path for the extra current maintained by the parasitic inductance of the main busbar, helping to reduce the overshoot voltage across the device. *C7* can be easily discharged to *C1* and *C2* through the inductor. Fig. 8*b* shows the two paths for discharging the other two capacitors – *C5* and *C6* in the snubber circuit. *C5* can be discharged through *C2*, *D4* and *D5*, but *C6* can be discharged through *C1*. The series connection of *D4*, *D5* and *D6* is in parallel with the main diode *D1*. The forward voltage drop of the main diode *D1* is relatively higher than that of the low-current diodes. The reason to put *D4* and *D5* in series is to ensure that most of the steady state input current goes through the main diode *D1* instead of *D4*, *D5* and *D6*.

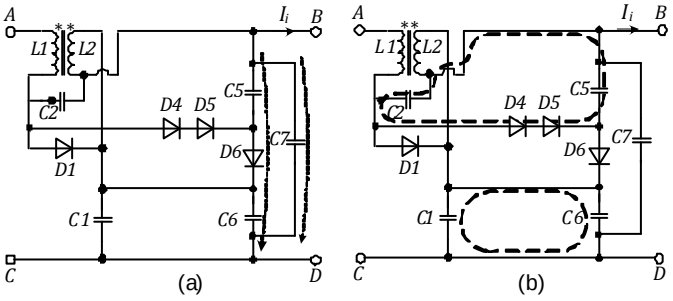


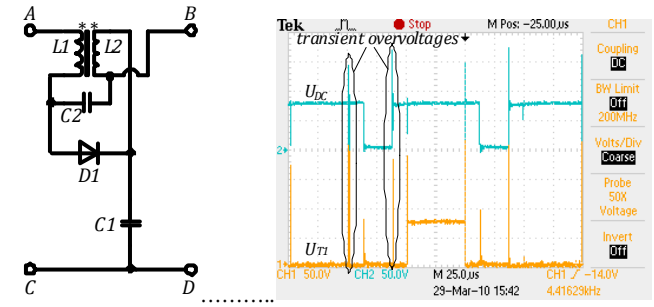
Fig. 8. The proposed DC-rail snubber circuit: charging loop (dashed arrows) (a), discharging loop (b).

The capacitor *C7* will cause extra loss during the shoot-through, therefore the capacitance of this capacitor has to be very small.

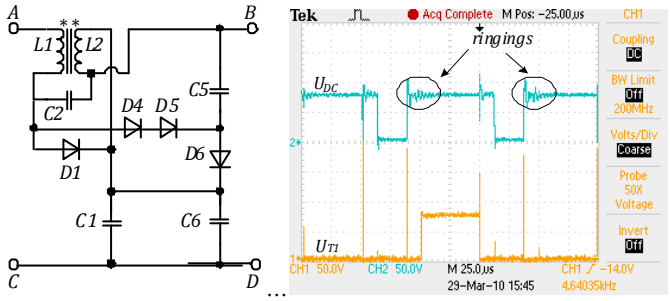
To provide a clear picture of the effect of snubber circuit, the three qZS-network circuits with respective waveforms of the DC-link voltage (U_{DC}) and voltage of one inverter switch (U_{T1}) are depicted in Fig. 9.

Fig. 9*a* presents the qZS-network without the snubber circuit. As shown, the transistor voltage overshoots can reach even 2.5 pu values during inverter operation. In addition, each change that occurs in an inverter switch results in overvoltages in the DC-link voltage (U_{DC}).

Fig. 9*b* shows the qZS-network with the main snubber circuit. The effect of this snubber can be seen in U_{DC} and U_{T1} waveforms. As shown, the dc-link voltage now is overvoltage free and high voltage stresses on transistor *T1* during switching are also reduced.



(a)



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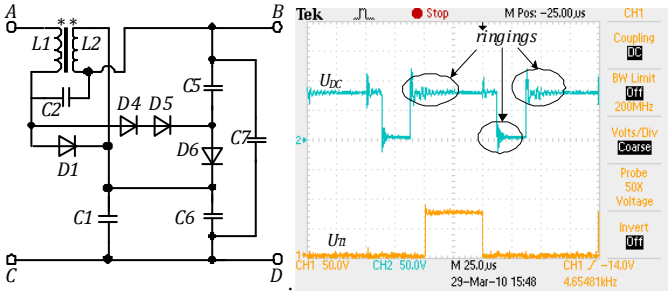

(c)

Fig. 9. qZS-network without snubber circuit (a), qZS-network with snubber circuit (b) and qZS-network with the snubber circuit and with an extra capacitor along the DC-link (c).

However, the drawback of capacitor use in the snubber circuit is shown by means of ringings that appear when the snubber circuit is used.

In addition, it can be seen that some transient overvoltages are still present in the U_{T1} waveform. This fact leads to the necessity to include an extra element (capacitor *C7*) in the snubber circuit along with the DC-link, as shown in Fig. 9*c*. It is apparent that an extra capacitor makes the U_{T1} waveform transient overvoltage free. However, as it was observed above (Fig. 9*b*), an extra capacitor has also a negative impact on the DC-link voltage. It causes additional voltage ringings in the U_{DC} waveform during switching-on and switching-off.

Selected elements for building snubber circuit in our converter prototype are given in Table VI.

TABLE VI
SELECTED ELEMENTS FOR SNUBBER CIRCUIT

Device	Specification
C5, C6	(Rifa PHE450MF7100JR06L2), polypropylene 630V, 1 µF
C7	(Wima FKP1T022206B00), polypropylene 650~V, 0.022 µF
D4, D5, D6	(International rectifier 30EPH06), Hyper fast diode 600V, 30A, V_F=1.8V, TO247

V. CONCLUSIONS

This paper presents practical design guidelines for a new step-up DC/DC converter topology for distributed power generation. The converter is intended for applications with widely changing input voltage, e.g. fuel cells or photovoltaic.

The converter consists of a voltage-fed quasi-Z-source inverter with continuous input current, a high-frequency step-up isolation transformer and a voltage doubler rectifier.

Major considerations for practical design of the proposed converter can be listed as follows:

- the converter performs the voltage step-up function and in some applications the input voltage could be gained more than ten times. It means that very high currents could circulate in the qZS-network and the PWM inverter. To minimize the undesired power dissipation special attention should be paid to component interconnections, especially to sizing of the wire cross-section. Implementation of laminated copper busbars is highly recommended;
- the diode *D1* should be selected in accordance with the operating frequency: twice and the same as the fundamental frequency of the isolation transformer. The Power Schottky diodes could be recommended for the *D1*;
- power switches with high operation frequency and low voltage drop should be selected in order to reduce the losses of PWM inverter.
- power losses in qZSI switches largely depend on the control system and the method. If power switches are commutated in soft switching mode, then only conduction losses are present, but if power switches are commutated in the hard switching mode, then dynamic losses can comprise up to 45% of the total losses.

- caused by transient processes the high transient overvoltages could occur on the capacitors of the qZS-network and snubber circuit. To increase the reliability and operation flexibility the polymer film capacitors could be recommended;
- accurate design of the coupled inductor can both increase the power density of the converter and provide material economy and reduce active power losses in the windings and in the magnetic core;
- a specific problem of the qZSI is the voltage overshoots across the inverter bridge caused by the stray inductance of the inverter supply circuit. To minimize the overshoots the multilayer copper busbars are highly recommended;
- implementation of snubber circuits can significantly eliminate high voltage stresses on semiconductor switches, but it causes high frequency ringings after switching (on/off) that will increase conduction losses in semiconductors and cause EMI. Further detailed research in this area is required;
- to increase power density of the converter, the operation frequency should be increased.

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