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Finite Element Analysis of Modular Pulse Width Modulation Converters with JAMG Software

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***Abstract* – The paper is devoted to half-bridge versatile power modules which can compose various converters. Successful use of such modules is possible if their construction is optimal from the electromagnetic and thermal points of view. The first purpose can be achieved utilizing bus-bars in the system of conductors. This ensures reduction of stray inductance, losses and module dimensions, as well as increase of switching frequency. Calculation of stray inductances is not an easy task which, however, can be successfully done with dedicated Finite Element Method (FEM) calculation software, for example JMAG. It can also be used for thermal calculations. In the given paper this method is applied to the analysis of a novel optimized design of the half-bridge module with concentrated DC-bus capacitors. The benefits of the module are shown with the help of simulation as well as experimentally. It is, however, stated that physical parameters of the module could be improved by splitting the DC-bus capacitors. The obtained design is more compact, but, as it was verified by means of simulation, also attractive from other points of view (EMC, voltage spikes, losses etc.). This design, therefore, can be recommended for future research.**

***Keywords* – Pulse width modulation converters, electronics packaging, electromagnetic interference, finite element analysis.**

I. Introduction

A variety of converters for different applications often includes the same repetitive stage – couple of series connected transistors and associated capacitors – transistor half-bridge. That is why the idea to build power electronic converters of the half-bridge modules seems quite obvious – [1], [2] and [3].

At the same time the current tendencies of power electronic converters development are the increase of their switching frequency and the reduction of their weight and size. However, such frequency increase is not possible at higher values of parasitic inductances because then the turn-on and turn-off switchings of MOSFETs and IGBTs are much slower. This causes significant losses in switches during transients and generation of huge amount of heat. Then it is necessary to install a bulky cooling system for heat dissipation, which can occupy a half of converter's size. Therefore reduction of the parasitic inductance: 1) improves EMC of the designed converter – [4], [5] and [6]; 2) reduces switching times, voltage peak values, switching losses and size of the cooling system – [7], [8] and [9]; 3) allows increasing switching frequency and reducing size of necessary passive components [10]. These and some other benefits can be achieved with implementation of the bus-bars – [11], [12].

In the half-bridge module parasitic inductance decreases maximally at full symmetry of conductors [4]. Full symmetry requires placing capacitors and switches one under another. At the same time capacitors with good equivalent series resistance (ESR) and equivalent series inductance (ESL) have larger size. For example, the 1000μF capacitors with ESR 60mΩ, ESL 16nH and for 450V have approximate dimension of 50mm x 100mm. Placing such capacitors one under another creates very bulky and inconvenient construction. Therefore, it is advisable to use a distributed system of capacitors. This gives reduction of total ESL, as well as optimization of elements layout, but increases the cost of the converter.

It is also essential to place the elements as close as possible to each other to keep the parasitic inductance low. This, however, decreases the capacitance of the bus-bars that requires more EMI filtering. Therefore a trade-off between maximum inductance reduction and improving of EMI filtering has to be found. One solution of this contradiction, that utilizes multilayer bus-bars with ground layer, is given in [13]. Taking all the above mentioned features into consideration makes calculation of optimal construction of the half-bridge module conductors quite complicated and time consuming.

Nowadays these bulky and time consuming calculations can be made with the dedicated software (though some alternative calculation methods also exist – [14]). In this research the design of all possible construction shapes was made with "SolidWorks" software, current conductive path simulation with Finite Element Method (FEM) – with "JMAG Designer" and "JMAG Studio" software, but overvoltage simulation – with "LTSpice".

The main purpose of this work is to improve the previously designed half-bridge module applying bus-bar principle and utilizing JMAG software for their calculation with FEM. The main goal during this optimization is the reduction of switching overvoltage.

II. Current Paths in Half-Bridge Module

There are two states of the half-bridge module: 1) active state, when current path is provided by one of the transistors of the module; 2) freewheeling state when the current path is provided by a diode. The operation of particular transistors and diodes depends on the polarity of the load current. Of course zero current state is also possible, but the role of parasitic parameters in this mode is less significant.

The current paths of the half-bridge module are shown in Fig.1. In the active state, Fig.1(a), the positive current path includes internal and wiring inductance of the conducting transistor ($L_{\sigma T1}$), of the upper, energy supplying, capacitor ($L_{\sigma C1}$) and of DC bus connections ($L_{\sigma W1}$). When the transistor

VT1 turns off current changes in this loop leads to significant overvoltage. In the freewheeling state, Fig.1(b) the positive current path includes internal and wiring inductance of the conducting diode ($L_{\sigma D2}$), of the lower, energy absorbing, capacitor ($L_{\sigma C2}$) and of DC bus connections ($L_{\sigma W2}$). Since the diode is not an active device these inductances do not lead to overvoltage. However, when the VT1 turns on, they slow down the switching process and leads to higher switching losses. The similar current paths can be found also for negative output current - Fig.1(c) and Fig.1(d).

With the opposite polarity the load current paths looks similar but all their elements are symmetrically different. Then a brief analysis can show that the inductances of capacitors ($L_{\sigma C1}$ and $L_{\sigma C2}$) and those of DC bus connections ($L_{\sigma W1}$ and $L_{\sigma W2}$) have impact on all switching transients. The latter inductance is smaller if the construction of conductors is optimal.

III. Basics of Inductance Calculations

Inductance L can be expressed as a ratio of magnetic flux change $d\Phi$ to the change of current di leading to the flux change [15]:

$$L = \frac{d\Phi(i)}{di}. \tag{1}$$

In turn, the elementary magnetic flux $d\Phi(i)$ may be found as a product of elementary surface dS and normalized induction B_n across this surface. Then the magnetic flux may be found as a surface integral:

$$\Phi(i) = \int_S B_n ds. \tag{2}$$

The normalized induction B_n is also an integral value and can be found based on the elementary magnetic induction dB produced by an elementary wire dl with current i found from Biot-Savart-Laplace law:

$$dB = \left| \frac{\mu_0 \mu_r}{4\pi} \cdot \frac{i \cdot \left[d\bar{l} \cdot \bar{r} \right]}{r^3} \right| = \frac{\mu_0 \mu_r}{4\pi} \cdot \frac{i \cdot dl \cdot \sin\theta}{r^2}. \tag{3}$$

In (3) μ_0 is magnetic permeability of vacuum; μ_r – relative permeability of material; r – the length of the radius-vector of the point where dB is calculated with respect to elementary wire position; θ – the angle between the radius vector and the elementary wire vector aligned with the direction of the current i. The induction B_n then can be found as a curve integral:

$$B_n = \int dB = \int_l \frac{\mu_0 \mu_r}{4\pi} \cdot \frac{i \cdot \sin\alpha}{r^2} dl. \tag{4}$$

Equations (1) to (4) produce exact value only for simple current paths the shape of which can be analytically described. Otherwise only approximate calculations with FEM are possible. For this reason the proposed solutions were calculated with “JMAG” software which utilizes FEM.

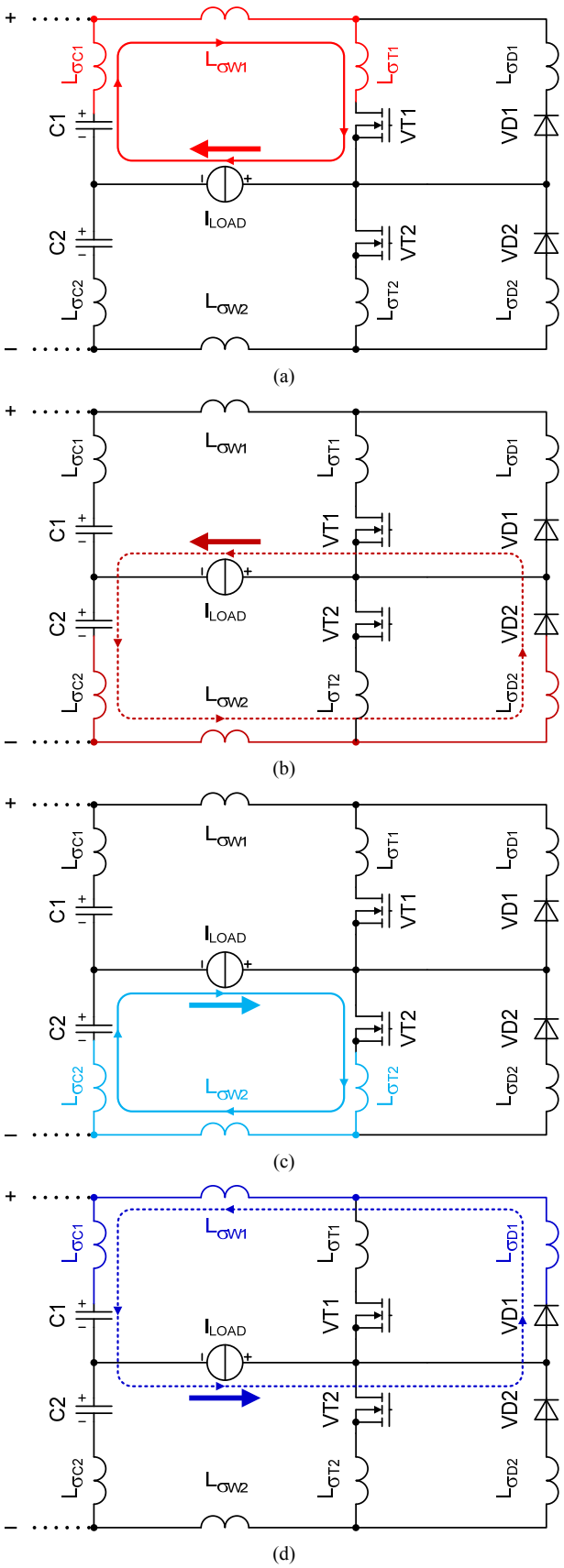


Fig.1. Current paths in half-bridge power module: (a) active current path for positive output current; (b) freewheeling current path for positive output current; (c) active current path for negative output current; (d) freewheeling current path for negative output current.

TABLE I. ELEMENTS OF THE MODULE

Element	Value	Stray inductance of element
RIFA Capacitor PEH200	1000uF	16 nH
Transistors IRF640	200V, 18A (switching frequency 20kHz)	12nH

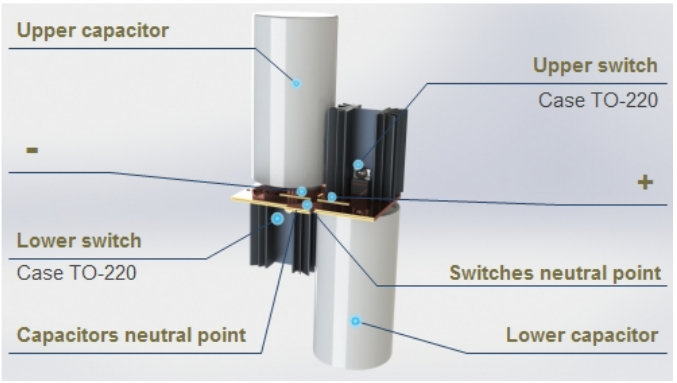
IV. Possible Designs of the Conductor System

A. Elements of the Module

The developed bus-bar designs were applied in a low voltage half-bridge module. The capacitors that were used in module are described in Table I.

The initial power board was not very successful due to its common (non bus-bar) design, distant placement of the main components, as well as due to its non-symmetry.

In order to overcome these drawbacks, the bus-bar approach and principles of symmetry in the half-bridge modules have been applied. Later, taking into account the symmetry principles, two different models were proposed.



(a)

(b)

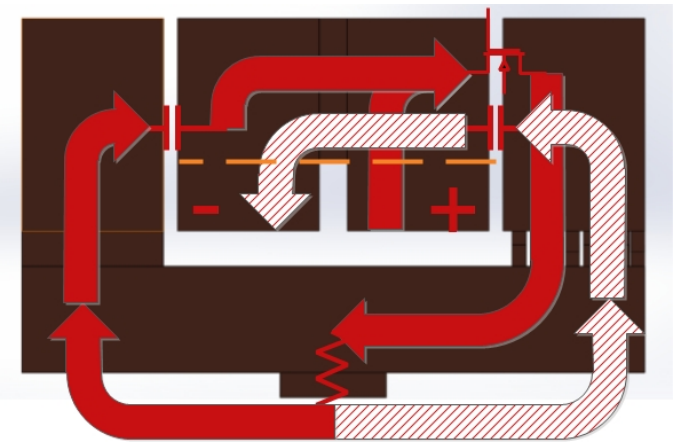
(c)

Fig.2. Views of module with concentrated capacitors: (a) details of constructions (SOLID-STATE model); (b) power part; (c) power part with attached driver.

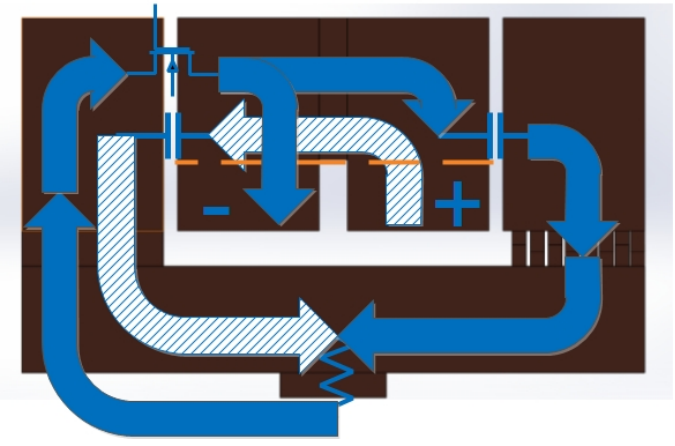
B. Symmetrical Bus-Bars for Half-Bridge

As it is stated in [4], [16] and [1], the principle of bus-bars assumes placing of one thin planar conductor, which conducts forward current, as close as possible to another one, which conducts the return current. However, usually there are two current paths – active and freewheeling. Moreover, in the half-bridge modules there are two DC-link capacitors and each has its own active and freewheeling path.

The symmetry of design (Fig.2) assumes that the active paths for both capacitors, as well as both freewheeling paths are equal. It is also very desirable to achieve the freewheeling path as similar as possible to the active path. It is obvious then, that the DC-link of the half-bridge converter is the most critical point for the providing the symmetry. The upper schematic elements of the half-bridge (C1, VT1 and VD1) are located on the top, while the lower schematic elements (C2, VT2 and VD2) – on the bottom of the module. Therefore, it has volume symmetry in respect to an axis situated in the conductor plane. In Fig.2 it is seen that the distance between capacitors and semiconductor modules has been reduced to the minimum and it is limited only by the physical dimensions of these elements. However, even in this short path the current goes through the symmetrical bus-bar. Thus this design provides the minimal value of parasitic inductance.



(a)



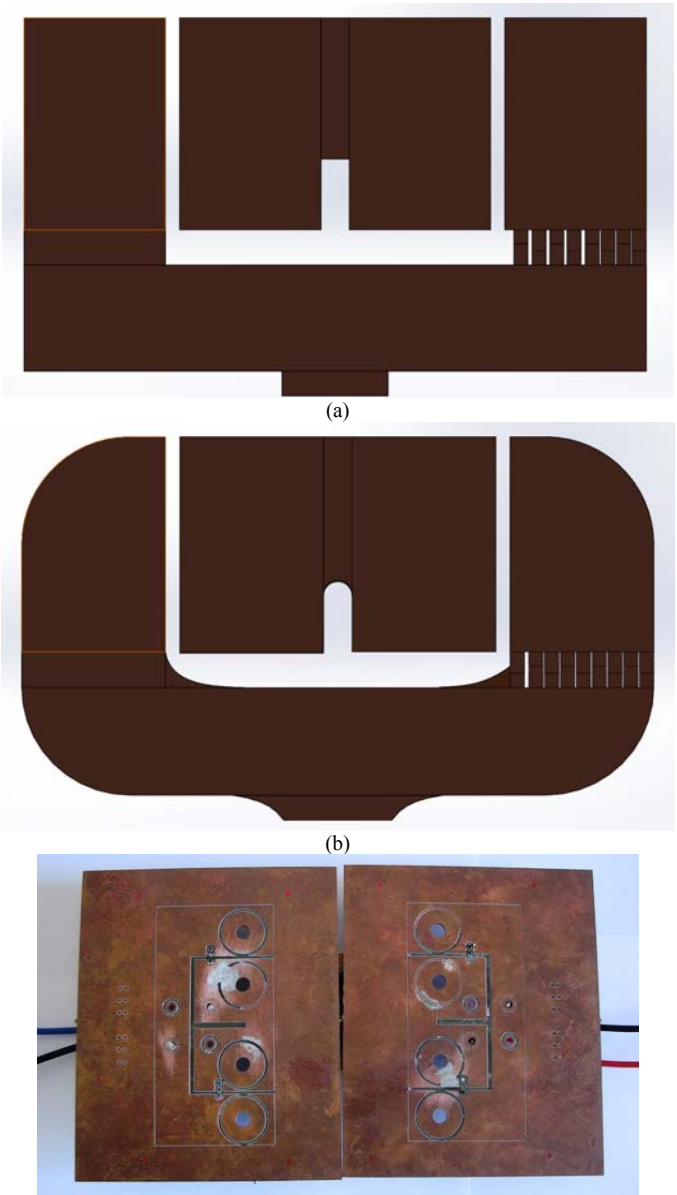
(b)

Fig.3. Expected active current paths in the proposed designs of half-bridge power module: (a) for positive output current; (b) for negative output current.

The expected active current paths for the second proposed design (the first one is quite similar) are shown in Fig.3 (where current directions correspond to Fig.1). In this figure solid filled arrows – are parts of the current path located on top side, but dashed ones – on the opposite. It can be seen that forward and return currents flow in the parallel bus-bars. Therefore, the corresponding expected inductance must be lower.

V. Minimizing of Stray Inductances with FEM Software

In order to check the proposed designs a series of simulations have been made. First of the all, the stray inductance of the proposed designs has been calculated with JMAG and the conductors shape has been optimized. Then the obtained inductance values were applied to a LTSpice simulation.



(a)

(b)

(c)

Fig.4. Current conductive copper planes of half-bridge module with concentrated capacitors: (a) first choice; (b) optimized for lower stray inductance; (c) opened bus-bar structure (the first choice).

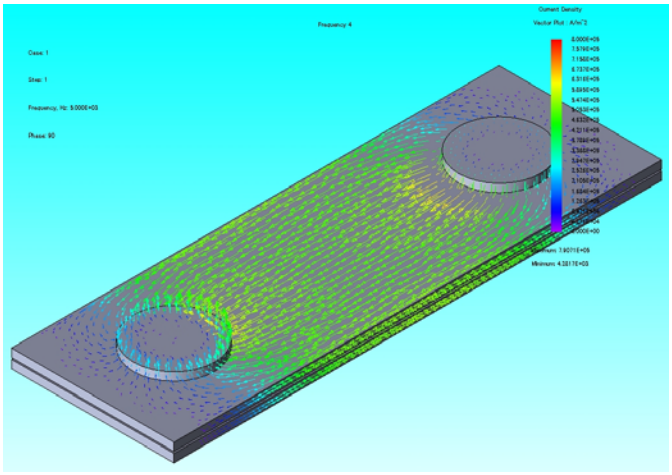
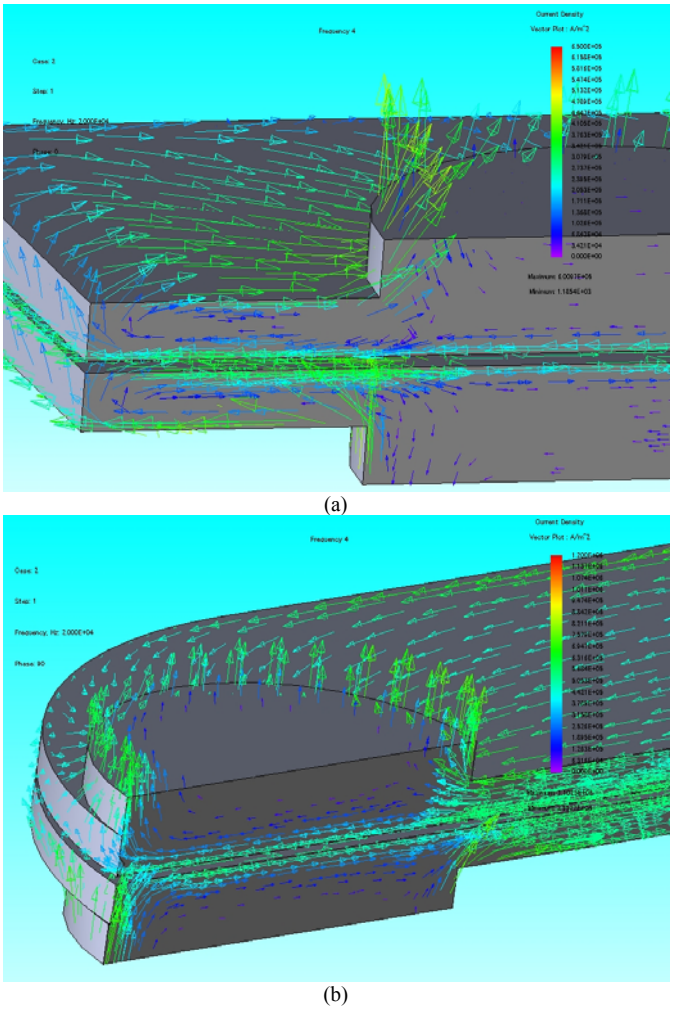


Fig.5. Simplified configuration of bus-bars for tentative analysis.



(a)

(b)

Fig.6. Cross-section of simplified bus-bars configuration: (a) non-optimized bus-bars and (b) optimized rounded bus-bars.

A. FEM in JMAG Designer and Studio

The analysis of complex bus-bars requires applying FEM. Such possibility is available in simulation software package that includes “JMAG Designer” and “JMAG Studio”.

The geometry file was exported in to "JMAG Studio" tool called «Calculate Bus-bar Inductance» from "SolidWorks" for mesh generation and specifying conditions of simulation such as: current inflow and outflow surfaces.

The bus-bar inductance calculation was made for the most important design versions: initial design without bus-bar (250nH), symmetrical non-optimized bus-bar design given in Fig.4(a) (43.0nH) and symmetrical optimized design with concentrated capacitors shown in Fig.4(b) (39.1nH).

Before optimization, several simulations with different shapes of bus-bars were made. In order to simplify these tentative simulations and to increase their speed a very simple configuration of conductors was chosen (two straight conductors – Fig.5).

Fig.6(a) shows the cross-section of the bus-bars given in Fig.5 with the corresponding magnetic field. The value of inductance found during this simulation is 16.4nH. In turn, the simulation of optimized rounded bus-bars presented in Fig.6(b) showed the inductance of 14.8nH. So, for the given configuration the optimization of the bus-bars shape has reduced the stray inductance by 10% [18]. For his reason the similar approach was applied to power board design of the half-bridge module.

As the result, although the bus-bar effect in the first module design is very strong, the module still can be improved – the corresponding non optimized simple designs have 7…10% higher stray inductances than the optimized one.

VI. Experiments with Bus-Bar Designs

Experiments have also been conducted for three prototypes of converters. All parameters and conditions of experiments were as equivalent as possible: supply voltage 30V DC, active load 100Ω with series inductance 3μH and switching frequency 20kHz.

The oscillograms of the first, not optimized, prototype are given in Fig.7(a). It is clear that even a good quality assemblage, without bus-bars yield bad results. The overvoltage is 53.1% that coincides with the corresponding simulation (see section VII for details) and is obviously an unacceptable result.

The second experiment was made with existing half-bridge converter with non-symmetrical non-optimized bus-bars is presented in Fig.7(b). The given converter has yielded rather good results of 25.2% overvoltage.

The third tested prototype with symmetrical bus-bars produces the results given in Fig.7(c). It produces overvoltage of 12.3%.

So, the experiments not only show the obvious bus-bar design benefits, but also the effect of optimization made with a help of JMAG.

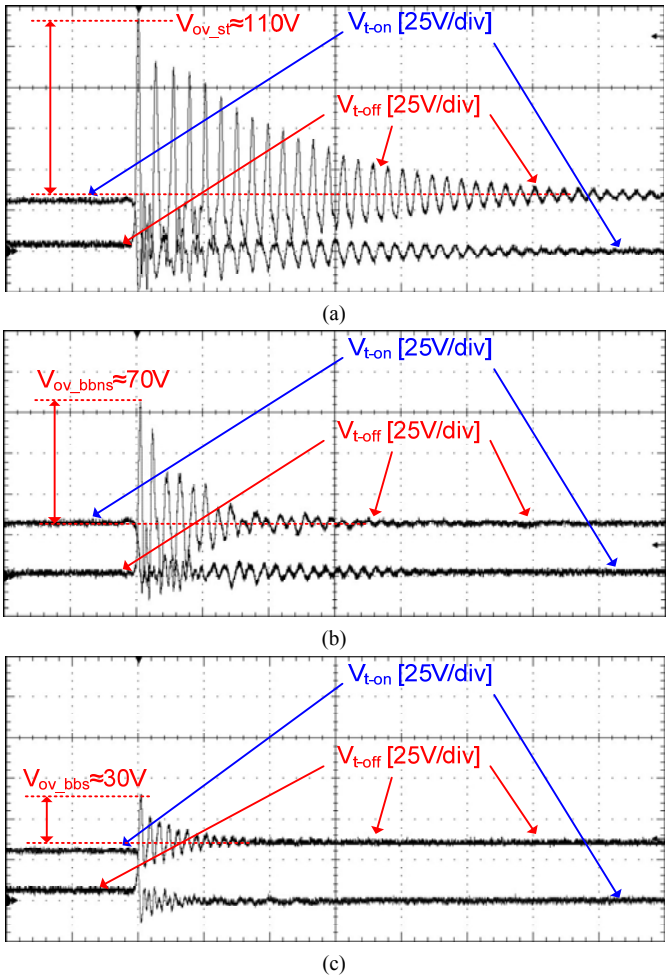


Fig.7. Experimentally obtained oscillograms of switching transients (time scale 200 ns/div, voltage scale 25 V/div, red – outgoing transistor, blue – incoming transistor): (a) without bus-bars; (b) with non-symmetrical bus-bars; (c) with symmetrical optimized bus-bars.

VII. Discussions and Future Works

A. Bus-Bars for Module with Distributed (Split) Capacitors

The main drawbacks of the design presented in Fig.2 are the inconvenient layout and height. In order to overcome these drawbacks one more design has been proposed. In this design the necessary capacitance is achieved with multiple capacitors. Moreover, the design with split capacitors has been optimized with the help of JMAG software.

The design with split capacitors achieves the balance between reduction of parasitic inductance, bus-bar capacitance increase and compactness. Several low-profile capacitors connected in parallel help to reach a more convenient placing of the converter's elements in space (Fig.8). Then the overall design is more "cubic" – i.e. equalized in all space dimensions.

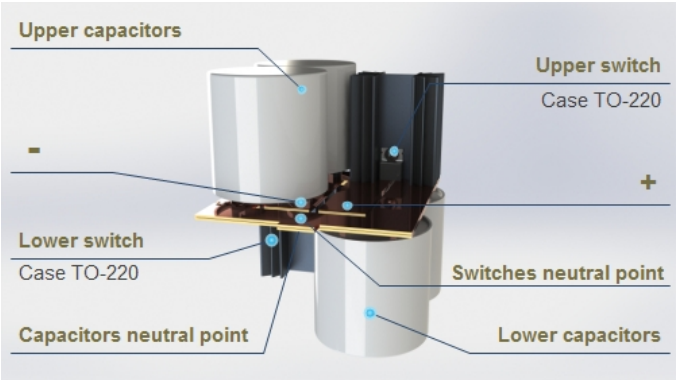


Fig.8. General view of module with split capacitors.

The parallel configuration of capacitors has ambiguous effect on the stray inductance. On one hand, parallel connection of capacitors helps to reduce the overall ESL of capacitor's pack:

$$L_{\Sigma} = \frac{1}{\sum_{k=1}^{N} \frac{1}{L_k}}. \qquad (5)$$

ESL of good capacitors is about 12-16nH and is more or less equal for the 1000μF and 470μF capacitors. Therefore the overall ESL of two 470μF capacitors with value will be 6nH. However, despite obvious reduction of the general ESL, the price of the given construction multiplies. The main reason - the price of 1000μF and 470μF capacitors with the same values of ESR and ESL is almost identical. The same overall ESL can be achieved also with cheaper capacitors. Unfortunately, ESR of such cheap capacitors can be inadmissibly big. Therefore a successful design requires an optimal trade-off between the improvement of ESR, ESL parameters and price of the capacitors.

However, on the other hand, the parallel placement of capacitors increases the current paths in the module. This, in turn, increases the stray inductance of the conductor system.

In order to find, which of these two tendencies is stronger one more series of JMAG calculations was done. The value 69.4nH has been obtained. So, the increase of the stray inductance (69.4 – 39.1 = 30.3nH) is higher than the reduction due to the parallel placement of the capacitors.

B. Analysis of Overvoltage with LTSpice.

The inductance values obtained with JMAG (69.4nH) were used during LTSpice simulation utilizing the built-in SPICE model of IRF640 MOSFET. The topology of the simulated half-bridge circuit is shown in Fig.9. The results of simulation are displayed for three inductance values: 1) 250nH; 2) 69.4nH and 3) 39.1nH (Fig.10). The parasitic inductance of 250nH leads to 47% overvoltage. It is obvious that such overvoltage during transient time can damage MOSFET if rated voltage is too low. Besides a serious EMI noise is created and the big losses during the switching.

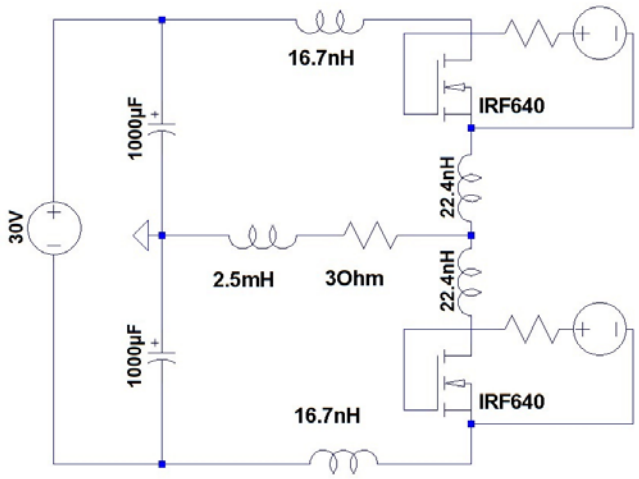


Fig.9. Equivalent schematic for LTSpice simulation.

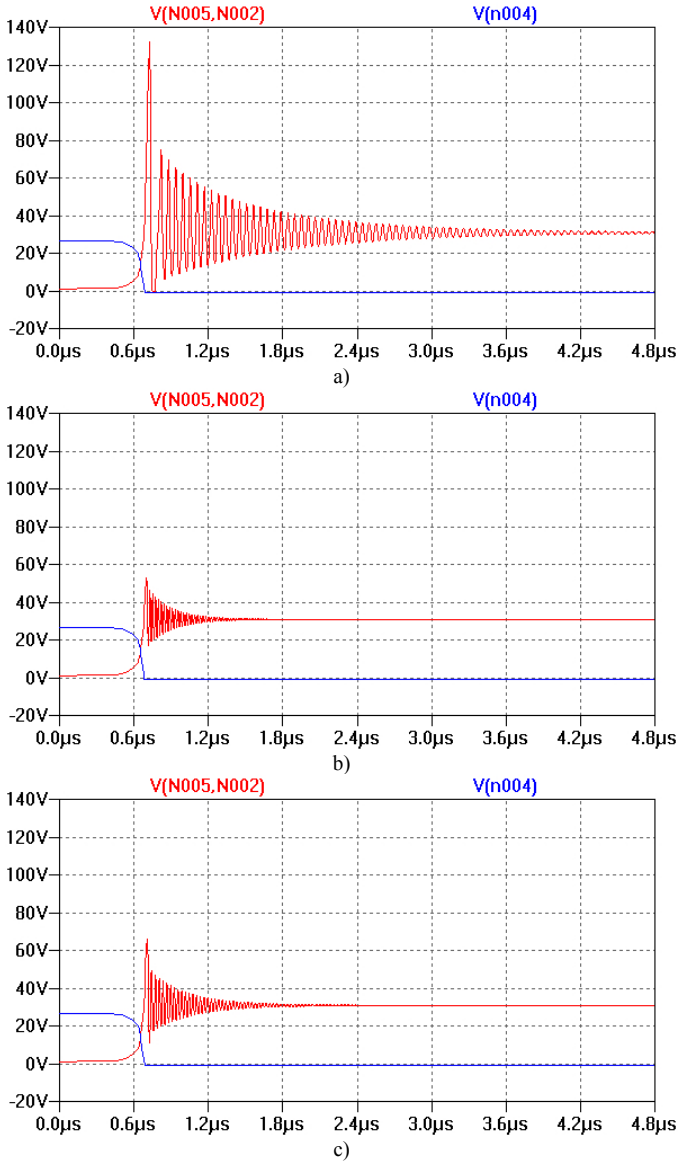


Fig.10. LTSpice simulation of switching transients (red – outgoing transistor, blue – incoming transistor): a) initial design with stray inductance 250nH; b) bus-bars for design with concentrated capacitors (39.1nH); c) bus-bars for design with split capacitors (69.4nH).

In the case of the stray inductance of 39.1nH which can be reached using the first bus-bar model (for concentrated capacitors) the overvoltage is only 10.2% that is considerably lower compared with other results. So, the simulation results show that the proposed designs could be successful.

The most significant conclusion, which follows from Fig.10 is that from the point of view of switching the design with split capacitors is not much worse than the design with concentrated ones. It could be used since it has other benefits.

It has also to be noted that this model is intended for tentative evaluation and it is not very detailed. For example, the analysis of comparable occasions in Fig.7 and Fig.10 shows that the real prototype has better oscillation damping compared with simulation. This difference can be explained by assumptions of the model which does not take into account all resistances of elements, for example, wire resistance. In fact in this model only the transistors are quite carefully described.

VIII. Conclusions

In this paper a bus-bar principle has been applied to the design of conductor system of a half-bridge power module, optimized with the help of FEM calculation software JMAG. Within this work two bus-bar designs of the half-bridge module have been proposed and optimized. One of them (with concentrated capacitors) has been comprehensively studied, while the second one (with split capacitors) looks promising and is scheduled for future research.

The overall conclusion is that the bus-bar principle can be successfully utilized in the module and can significantly (more than by 10%) reduce the switching overvoltage. One more conclusion gives preference to the conductors with rounded corners. It also has been noticed that significant trade-off between internal parameters of the DC-link capacitors, their capacitance and price has to be done in the optimal module design.

Although certain experiments were conducted, the obtained practical material was very limited. That is why more experiments are planned for the nearest future. First of the all they include experiments with high voltage transistors, as well as with SOT227 packages. Then split capacitor design has to be explored and the inductances of all designs have to be measured (at least indirectly, with frequency generator and spectrum analyzer). Also the impact of bus-bars on the module losses and its EMI has to be tested experimentally. Finally, the impact of bus-bars on the operation of several modules in different configurations has to be studied.

So, after all the experiments it can be concluded that the FEM software (JMAG) is an excellent tool not only for analysis of modular pulse width modulation converters, but also for their optimization.

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Ilya Galkin is IEEE member since 2006 in societies of Power Electronics, Industrial Electronics, Automatic control and Education.

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