Analysis of Transformerless Bidirectional AC/DC Converter Based on Double Half-Bridge Topology with Non-Commutating Neutral Wire

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***Abstract* –The present article studies the converter, which is based on dual half-bridge topology with common neutral wire that is not commutating during converter's operation. The current sensorless control algorithm has been obtained analytically for rectification, grid-tied and stand-alone inverter modes, which average value tracks reference current signal with constant switching frequency. Two control functions for inductor's discontinuous and continuous current modes have been defined for each of operation modes, and sensorless transition between two modes has been stated. The results of simulation in the PSIM software approved the analytical model, keeping the average inductor's current to follow the reference value in inductor's discontinuous and continuous conduction modes.**

***Keywords* – AC-DC power converters, sensorless control, current control, inverters, pulse width modulation converters.**

I. Introduction

The energy demand is growing at the rate of 2.4% annually [1] due to increasing Earth's population and standards of living, pushing countries to install new generation facilities at a regular base. While the consumption of fossil resources remain reasonable, countries also invest finances [2] into development of renewable energy sector, where the potential of hydro resources is almost utilized in some regions [3], the wind and Solar energy are getting into the focus – installing on-shore and off-shore wind parks and Solar plants. The increasing popularity of PV panels positively impacts the price for this technology, that is about 0.138-0.163 €/kWh for PVs plants in Germany [4]. Countries might also adopt their legislation concerning connection of small energy sources, so that people would become prosumers. Spectacular example of that is Denmark, where 36 MW of PV panels are connected to the grid monthly in residential sector, after allowance to "store" energy in the public grid surplus consumption [5].

At the same time grid modernization concepts are developed, such as microgrid [6] and nanogrid [7], which are targeted for superior functionality of local grids with higher efficiency and stability values. These concepts also promote the use of DC subgrids [8] which allows reducing energy conversion count, as a result reaching higher efficiency values [9]. The bidirectional AC/DC converter gets in focus, which is responsible for stability in both – AC and DC – subgrids.

This article is dedicated to analysis of transformerless dual half-bridge bidirectional AC/DC converter with common neutral point that is not commutating during converter's operation. It is reasonable for primary AC/DC energy transformation in household applications that allows eliminating AC/DC conversions, leaving only built-in DC/DC schemes with galvanic isolation (if needed) in end devices and improving their efficiencies.

The article is structured as follows: firstly, the sensorless current control algorithm with constant switching frequency is developed for rectification, grid-tied and stand-alone inverter modes; secondly, the calculations of LCL filter are made and adaptation of control algorithm is discussed; thirdly, two balancing circuits are analyzed and control issues are discussed.

II. Description of Topology

Various bidirectional topologies are proposed for intelligent grid applications, for instance: non-isolated converter with half-bridge that interfaces AC side and full-bridge interfacing DC side [10], DAB topology with non-resonant [11] or resonant [12] isolation stage. The first one is not safe for operation, because both terminals of DC grid are under high potentials, while two other are bulky due to the use of transformer.

Hereby, the authors would like to discuss the double half-bridge bidirectional interface converter with common neutral, which is not commutating during converter's operation that provides save utilization. As the DC side mostly charges and discharges the capacitor C1, the balancing circuit is introduced, which will be discussed in details later in section V.

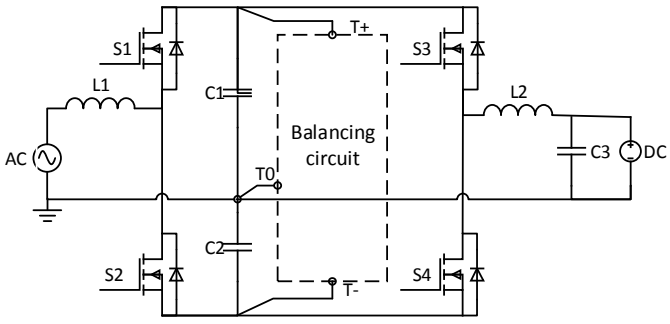

Fig. 1. Proposed bi-directional AC/DC converter's topology.

III. CURRENT CONTROL

A. Overview

A lot of current control techniques are known from literature [13], [14]: hysteresis, delta modulation, boundary switching, which are all relevant in some specific applications. On the other hand, input inductor's current sensing in high frequency switched mode power supply (SMPS) is the most challenging task, which also significantly increases the cost and size of control system as it was mentioned in various articles [15] [16]. Concerning the current control for proposed converter the constant switching current sensorless control technique is selected, as accordingly to [17], it reduces switching losses in comparison with variable frequency hysteresis control, as well as reduces high-frequency components. The comparison with other sensorless control approaches is provided in table I.

TABLE I

OVERVIEW OF DIFFERENT SENSORLESS CONTROL TECHNIQUES

		[18]	[19]	[20]	[21]	Proposed
Fixed switching frequency		√	√	√	√	√
Fixed-amplitude carrier		√	√			√
Current form	DCM					√
	CCM	√	√	√	√	√
Stable to non-sinusoidal input voltage			√		√	√
Current sensorless		√	√			√
Input voltage sensorless				√	√	

B. Rectifier mode

The typical operation half-bridge topology in active rectifier mode is shown in the figure below.

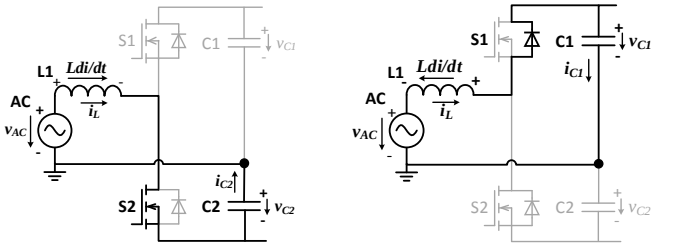

Fig. 2. Commutated current paths in rectification mode during positive half-wave of input voltage.

The current forms during one switching period are seen in the figure below.

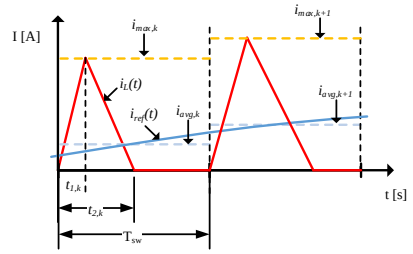

Fig. 3. Inductor's current form during single switching period in DCM.

Assuming that capacitor voltages remain constant during one switching period, but input voltage is averaged, inductor's maximal current is described by voltage applied to inductor *L1* during transistor's conduction time ($t_{1,k}$) and diode's conduction time ($t_{2,k}$-$t_{1,k}$) as:

$$i_{\max,k} = \frac{v_{C2,k} + v_{AC\_avg,k}}{L} \cdot t_{1,k} \quad (1)$$

$$-i_{\max,k} = \frac{v_{C1,k} - v_{AC\_avg,k}}{L} \cdot \left(t_{2,k} - t_{1,k}\right) \quad (2)$$

where L is input inductor inductance, V_{C1} and V_{C2} are capacitors' voltages, V_{AC_avg} is input sine-form voltage averaged during one switching period, but index k indicates discrete values during k[th] switching period.

The average inductor's current ($i_{avg,k}$) during one switching period (T_{sw}) is defined as:

$$i_{avg,k} = \frac{i_{\max,k} \cdot t_{2,k}}{2 \cdot T_{sw}} \quad (3)$$

Taking into account equations (1)-(3) the transistor's conduction time during DCM mode is defined as:

$$t_{1,k} = \sqrt{\frac{\left|i_{avg,k}\right| \cdot 2 \cdot L \cdot T_{sw} \cdot \left(v_{C1,k} - v_{AC\_avg,k}\right)}{\left(v_{C2,k} + v_{AC\_avg,k}\right) \cdot \left(v_{C1,k} + v_{C2,k}\right)}} \quad \textbf{(4)}$$

During CCM period another control law should be used, taking into account that $t_{2,k}$ now is equal to switching period T_{sw}. Transistor's conduction time can be extracted from equation below:

$$\frac{v_{C2,k} + v_{AC\_avg,k}}{L} \cdot t_{1,k} + \frac{v_{C1,k} - v_{AC\_avg,k}}{L} \left(T_{sw} - t_{1,k}\right) = \Delta i_{ref,k}, \quad (5)$$

which can be explained as integral of voltage applied to inductor during one switching period that is equal to reference current discrete change during one switching period (Δi_{ref}). So that the control law for CCM period is defined as:

$$t_{1,k} = \frac{\Delta i_{ref,k} \cdot L + \left(v_{C1,k} - v_{AC\_avg,k}\right) \cdot T_{sw}}{\left(v_{C1,k} + v_{C2,k}\right)} \quad (6)$$

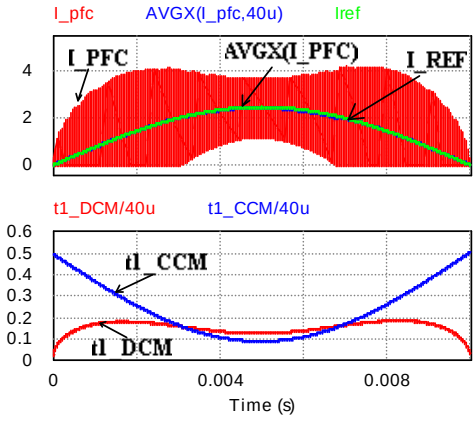

Fig. 4. Simulation result for rectification mode.

The simulation in PSIM software was made in order to evaluate obtained control laws. The figure above demonstrates two graphs with current forms (top graph) and both control

laws (bottom graph). Inductor's *L1* current (red) is seen on top graph of Fig. 4, the average current of which (blue) is the following reference current form (green). The bottom graph represents DCM and CCM timing functions, which cross at boundary conduction mode. The control system chooses minimal value between (4) and (6) to control the transistor.

C. Grid-tied inverter mode

The grid-tied inverter mode is analyzed similarly to rectification mode, concerning that S1 transistor is commutating during positive half period of input voltage.

Thus, the control law for DCM is defined as:

$$t_{1,k} = \sqrt{\frac{\left|i_{avg,k}\right| \cdot 2 \cdot L \cdot T_{sw} \cdot \left(v_{C2,k} + v_{AC\_avg,k}\right)}{\left(v_{C1,k} - v_{AC\_avg,k}\right) \cdot \left(v_{C1,k} + v_{C2,k}\right)}}, \quad (7)$$

while inductor's current in CCM is controlled by using the following definition, which is obtained in the same way as in (6):

$$t_{1,k} = \frac{-\Delta i_{ref,k} \cdot L + \left(v_{C2,k} + v_{AC\_avg,k}\right) \cdot T_{sw}}{\left(v_{C1,k} + v_{C2,k}\right)}. \quad (8)$$

D. Stand-alone inverter mode

The stand-alone inverter mode requires different control law than in grid-connected mode, as capacitor's voltage on one side and voltage drop on the load from another side are balanced with electromotive force of input inductor. As a result inductor's *L1* current is changing in exponential way.

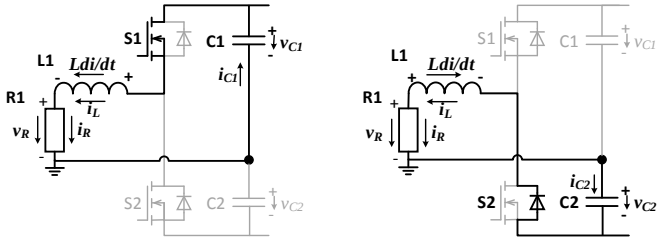

Fig. 5. Commutated current paths in stand-alone inverter mode during positive half-wave of generated voltage.

Two equations below ((9) and (10)) describe the rising and falling current forms:

$$i_L(t) = \int_{t_{0,k}}^{t_{1,k}} \left(-v_{C1}(t) - R \cdot i_L(t)\right) dt,\ t \in \left[t_{0,k}, t_{1,k}\right] \quad (9)$$

$$i_L(t) = \int_{t_{1,k}}^{t_{2,k}} \left(v_{C2}(t) - R \cdot i_L(t)\right) dt + i_L\left(t_{1,k}\right),\ t \in \left[t_{1,k}, t_{2,k}\right] \quad (10)$$

where *R* is load resistance.

Solving differential equations above the following results are obtained:

$$i_L(t) = -\frac{v_{C1,k}}{R} \cdot \left(1 - e^{-\frac{R}{L} \cdot t}\right),\ t \in \left[t_{0,k}, t_{1,k}\right] \quad (11)$$

$$i_L(t) = \frac{v_{C2,k}}{R} \cdot \left(1 - e^{-\frac{R}{L}(t - t_2)}\right),\ t \in \left[t_{1,k}, t_{2,k}\right] \quad (12)$$

The $t_{2,k}$ timing function can be defined from (9) and (10) as follows:

$$t_{2,k} = -\frac{\left(v_{C1,k} + v_{C2,k}\right) \cdot t_{1,k} + R \cdot i_{avg,k} \cdot T_{sw}}{v_{C2,k}} \quad (13)$$

In order to obtain control law for stand-alone inverter mode, the (11) and (12) are equalized at time $t_{1,k}$. After rearranging variables the equation looks like:

$$\frac{v_{C2,k}}{v_{C1,k}} e^{-\frac{R}{L} \cdot t_{1,k}} = \left(1 - \frac{v_{C2,k}}{v_{C1,k}}\right) e^{-\frac{R}{L} \cdot t_{2,k}} - e^{-\frac{R}{L}\left(t_{1,k} + t_{2,k}\right)}, \quad (14)$$

that makes sense of transcendental function, as trying to extract natural logarithms from both parts, the timing function $t_{1,k}$ will be defined by natural logarithm that contains the same timing function. Thus, this equation has no algebraic solution, however, it could be simplified assuming that the ratio of voltages approximately equal to 1, and, secondly, the last part has smallest contribution to all equation, because of biggest absolute value of exponent, which due to negative sign tends to zero faster than other parts which contain exponent. Thus, the result of simplification is written as:

$$e^{-\frac{R}{L} t_{1,k}} = 2e^{-\frac{R}{L} \cdot t_{2,k}} \quad (15)$$

which in contrast to (14) has an algebraic solution. Taking into account $t_{2,k}$ definition from (13), the control law is defined as:

$$t_{1,k} = \frac{R \cdot i_{avg,k} \cdot T_{sw}}{v_{C1,k}} - \frac{v_{C2,k} \cdot L}{v_{C1,k} \cdot R} \cdot \ln\frac{1}{2} \quad (16)$$

The simplified control law is admissible at more or less equal capacitor voltages and relatively high resistance of the load, while precise control law can be obtained only by using numerical methods for solving transcendental equations, for example, bisection method. The figure below demonstrates graphical representations of simplified and precise control laws for 2.5 A amplitude of reference signal and 124.4 Ω of load. The graphs are almost identical, however, the difference is much noticeable at higher loads.

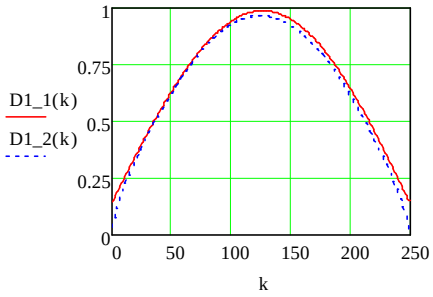

Fig. 6.Graphical representation of precise and simplified control laws for stand-alone inverter mode.

The control law for CCM is defined similarly as it was done previously for rectification or grid-tied inverter mode, resulting in:

$$t_{1,k} = \frac{-\Delta i_{ref,k} \cdot L + \left(v_{C2,k} + R \cdot i_{ref\_avg}\right) \cdot T_{sw}}{\left(v_{C1,k} + v_{C2,k}\right)}. \quad (17)$$

In order to verify obtained control laws for stand-alone inverter mode, the simulation in PSIM was made, where bisection method was implemented to obtain the transistor's conduction time during DCM.

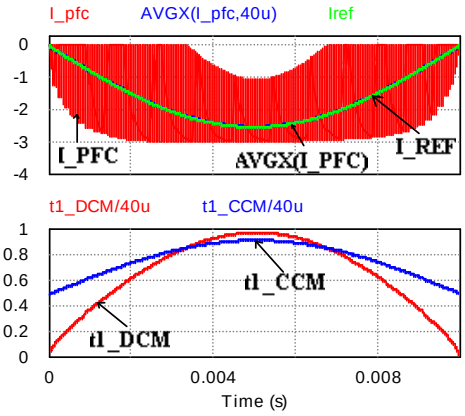

Fig. 7. Simulation result for stand-alone inverter mode.

IV. LCL Filter

As it was observed from simulations previously, the current consumed or generated into the grid hardly reminds the sine-form, because of high amount of higher harmonics located near converter's switching frequency. The LCL filter (see Fig. 8) commonly is used for reduction of harmonics, which require special care of calculation keeping trade-off between quality of input current and dimensions of the filter, which are also proportional to filter's price.

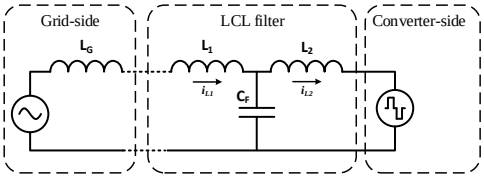

Fig. 8. Location of LCL filter.

A. Calculation

The converter-side inductor is selected by using boost converter's inductance selection equation, where current ripple is limited by capacitor's admissible ripple value. The ALC10A471DF450 capacitor is considered to be used in AC/DC converter with 4.03 A of allowed current ripple [22].

$$L_{F2} = \frac{\left(v_{C2,k} + v_{AC,k}\right) \cdot D_k}{f_{SW} \cdot \Delta I_{ripple}} \tag{18}$$

The filter capacitor is selected in order to shunt higher harmonic currents with the capacitor branch, selecting impedance of the capacitor lower than grid-side inductor's impedance (about 1/10 or 1/5 of X_{L_G}):

$$X_{CF} = \left(\frac{1}{10} to \frac{1}{5}\right) X_{L1} \tag{19}$$

If the constraint is not fulfilled and capacitor impedance is comparable with grid side inductor's impedance, the filter capacitor will not be able to shunt enough the current ripple and more distorted current will be injected to the grid. On the other hand – larger capacitance will result in increased reactive power flow. The reactive power limit is usually selected below 5% of system rated power [23]. Thus, the capacitance limit is defined as:

$$C_F \le 0.05 \frac{P}{2\pi \cdot f_{AC} \cdot V_{AC}^2} \tag{20}$$

where V_{AC} is RMS value of input voltage, P is rated power, f_{AC} grid's frequency. The C_F value of 1.6 µF is selected for 1 kW converter, which corresponds to 2.5% of rated converter's base impedance.

Another constraint is related to LCL filter self-resonance frequency, which is defined by the following equation:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_{F1} + L_{F2}}{L_{F1} \cdot L_{F2} \cdot C_F}} \tag{21}$$

The resonant frequency should match the following constraint:

$$10 f_{AC} < f_{res} < \frac{1}{2} f_{SW} \tag{22}$$

Selecting 0.2 mH for grid-side inductor both constraints ((19) and (20)) are fitted, as grid-side inductor's impedance is tenfold in comparison with selected filter capacitor impedance and LCL filter's resonance frequency (6 kHz) is located within the defined range (10*50 Hz < f_{res} < 25/2 kHz).

The figure below demonstrates the performance LCL filter, where the top graph represents converter-side inductor's current, while bottom graph corresponds to grid-side inductor's current.

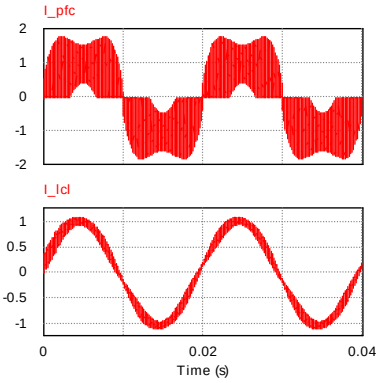

Fig. 9. Simulation results for evaluation of LCL filter.

The following table contains converter-side and grid-side inductors' current THD values obtained by simulation in PSIM at different input current reference values.

TABLE I

PERFORMANCE OF LCL FILTER

	I_M [A]	7.5	5	2.5	1	0.5
Rectifier mode	THD(I_{L2})[%]	13.6	19.5	34.9	67.3	101.2
	THD(I_{L1})[%]	1.8	2.7	4.5	8.2	11.5
Inverter mode	THD(I_{L2})[%]	12.1	17.7	32.4	63.8	96.1
	THD(I_{L1})[%]	1.7	2.5	4.4	8.2	11.5

B. Adaptation of proposed switching technique

Special consideration should be taken into account in order to use previously obtained control laws for converter's operation with LCL filter. During DCM mode only converter-side inductor should be taken into account to calculate the transistor's duty cycle for rectification and grid-tied inverter modes. During CCM the total inductance of the LCL filter should be considered to calculate transistor's conduction time for rectification and grid-tied inverter modes.

The stand-alone inverter's mode with LCL filter should be treated as grid-tied inverter mode as the current waveforms are not exponential, but linear due to filter capacitor.

V. Balancing Circuit

The proposed converter needs balancing circuit as output half-bridge mostly charges and discharges capacitor *C1*. Thus, the balancing circuit should provide half of the power required by output half-bridge. This balancing circuit can be implemented as hard-switched, either soft switched, as it is demonstrated in the figure below.

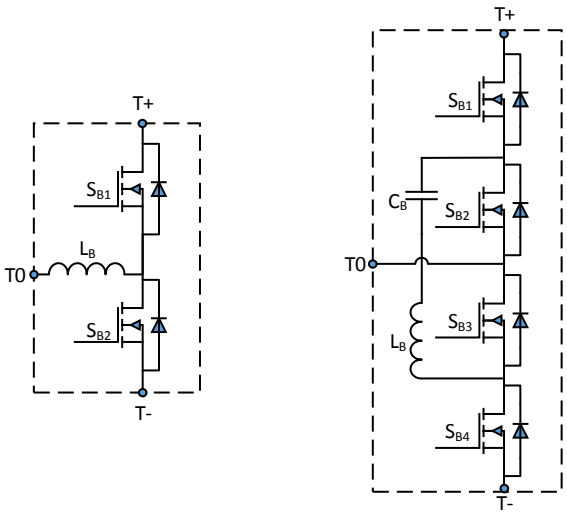

Fig. 10. Hard-switched (left) and soft-switched (right) capacitors' voltage balancing circuits.

A. Hard-switched balancing circuit

The hard-switched balancing circuit utilizes two semiconductor switches and additional inductor as energy storage element. In order to provide energy from capacitor *C2*, the S_{B2} switch is controlled. During S_{B2} conduction state energy is stored in the inductor L_B and, when the S_{B2} is switched off, stored energy is released to capacitor *C1* through diode of S_{B1}.

The control law for hard switched balancing circuit during DCM inductor's mode is defined similarly to (4) and (7):

$$t_{1,k} = \frac{\sqrt{i_{C2\_avg,k} \cdot 2 \cdot L_B \cdot T_{sw} \cdot v_{C1,k}}}{v_{C2,k}} \qquad (23)$$

B. Soft-switched balancing circuit

The soft-switched balancing circuit utilized resonant bank as energy storage and four semiconductor switches, controlling *SB3* and *SB4* during energy transfer from capacitor *C2* to capacitor *C1*, while *SB1* and *SB2* are represented by their diodes. Reversed energy transfer is possible commutating switches *SB1* and *SB2*.

The energy stored in resonant bank is equal to the energy of the charged resonant capacitor at the end of half-period:

$$E_{LC} = \frac{C \cdot v_{CB\_\max}^2}{2} \qquad (24)$$

The resonant inductor should be selected in order to provide resonant frequency, at which half of the output power should be supplied by resonant bank. The inductance of the resonant inductor can be found from:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_B C_B}} \qquad (25)$$

The table below contains parameters of resonant balancing circuit with calculated values of maximal power flow, amplitude current and resonant frequency.

TABLE II

Parameters of Resonant Balancing Circuit

Combination	C_B [nF]	L_B [uH]	f_{res}[kHz]	*I_M [A]	*P [W]
I	75	540	25	4.7	600
II	68	560	25.8	4.4	544
III	82	470	25.6	5.3	656

* - calculated for 25 kHz operation, $V_{C2}(0)$=400 V

The first combination of passive components was calculated for 600 W of balancing power, while the second and the third combinations are selected out of standard nominal values for passive components. Slightly higher resonant frequency is admissible, as time reservation for dead-band should be taken into account.

The diagram below demonstrates the performance of balancing circuit for the second solution from Table II, showing almost linear growth of transferred power depending on the voltage of discharging capacitor. Thus, the regulation of transferred energy depends on the delays that are inserted between switching periods and by controlling the voltage of discharging capacitor.

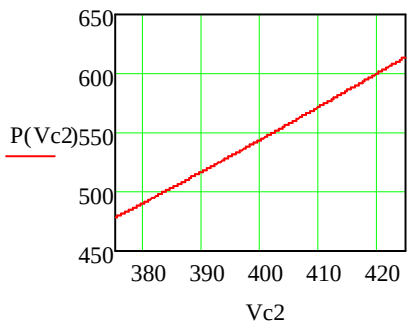

Fig. 11. Performance of resonant balancing circuit (C_B=68 nF, L_B=560 uH, f_{sw}=25 kHz)

VI. Conclusions

The proposed bidirectional AC/DC dual half-bridge converter has advantage over other solutions due to non-commutating neutral wire that eliminates also the use of transformer; thus, the power density of the converter can potentially be increased. The current sensorless control algorithm has lower cost and size of the control system in comparison with sensored control. Proposed algorithm has been obtained analytically and confirmed by simulations for all operation modes. The constant switching frequency potentially allows keeping the high performance of the LCL filter at wide range of power ratings. The soft-switched balancing circuit is more advantageous as it provides self-regulation function, as the higher is dischargeable capacitor voltage the more energy is transferred to chargeable capacitor.

Acknowledgements

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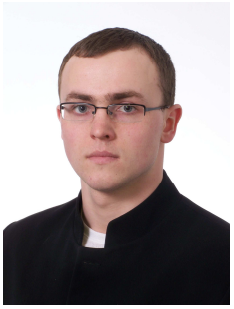

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