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MEASUREMENT AND MODELING OF EMI FILTERS HIGH FREQUENCY PARASITIC PARAMETERS

PhD thesis

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Annotation

PHD thesis is devoted to field of Electromagnetic compatibility (EMC) - the branch of electrical sciences which studies the unintentional generation, propagation and reception of electromagnetic energy in conductive form and as radiation, leading to unwanted effects- electromagnetic interference (EMI). This thesis covers one of the EMC aspects- filters- more precisely- EMI power filters modeling, measurements and analysis.

First chapter is devoted to overview of EMC topical problems and recent research in the field of EMI power filters.

Second chapter covers mathematical background used in thesis- S-parameter application in filter characterization, S- parameter relationships, inductive component analysis using vector network analyzer, capacitive component analysis using vector network analyzer and errors related to measurement methodologies.

Third chapter analyzes effects of parasitic component parameters on Π type three phase EMI filters. Three phase filter parasitic components are extracted using S- parameter measurement techniques.

Forth chapter analyzes effects of parasitic component parameters on T type three phase EMI filters. Three phase filter parasitic components are extracted using S- parameter measurement techniques.

Fifth chapter introduces novel EMI power filter capacitor modeling using CST MWS. Three capacitor models are developed to increase modeling speed and decrease required PC resources. Mutual coupling between two capacitors and mutual coupling reduction techniques are modeled and modeling results compared to measurements.

Sixth chapter covers EMI power filter inductor modeling using CST MWS. Inductors are successfully analyzed. Mutual coupling between two inductors and mutual coupling reduction techniques are analyzed using CST MWS. Modeling results are compared to measurement results.

PHD thesis is divided in six chapters and includes 161 figures, 7 tables, 113 equations, 53 cross references in literature, annotation in English and Latvian, introduction, table of contents and is written on 162 pages.

Anotācija

Promocijas darbs ir veltīts elektromagnētiskās savietojamības jomai, precīzāk, elektromagnētiskās interferences barošanas filtru modelēšanai, mērījumiem un filtra parazītisko parametru analīzei.

Pirmajā nodaļā tiek vispārīgi apskatīta literatūra un problēmas, kas saistītas ar elektromagnētiskās interferences barošanas filtru modelēšanu, mērījumiem un filtra parazītisko parametru analīzi.

Otrā nodaļa veltīta matemātisko sakarību izklāstam un skaidrojumam- S-parametru pielietojums filtru analīzē, S-parametru sakarības, induktīvo filtra komponenšu analīze izmantojot S-parametrus, kapacitatīvo filtra komponenšu analīze izmantojot S-parametrus un kļūdas, kas saistītas ar S-parametru pielietošanu.

Trešā nodaļa apskata trīs fāžu Π tipa filtru parazītiskos parametrus un to iespaidu uz filtra sniegumu. Izmantojot S-parametru mērījumus, tiek aprēķināti un analizēti trīs fāžu filtru parazītiskie parametri.

Ceturtā nodaļa apskata trīs fāžu T tipa filtru parazītiskos parametrus un to iespaidu uz filtra sniegumu. Izmantojot S-parametru mērījumus, tiek aprēķināti un analizēti trīs fāžu T tipa filtru parazītiskie parametri.

Piektā nodaļa ietver inovatīvu elektromagnētiskās interferences barošanas filtru kondensatoru modelēšanu, pielietojot CST MSW 3D elektromagnētisko lauku modelēšanas programmatūru. Izstrādāti trīs kondensatoru modeļi, kas samazina laiku un skaitļošanas resursus, kuri nepieciešami kondensatoru modelēšanai.

Sestā nodaļa veltīta elektromagnētiskās interferences barošanas filtru induktīvo komponenšu modelēšanai, pielietojot CST MSW 3D elektromagnētisko lauku modelēšanas programmatūru.

Promocijas darbs rakstīts angļu valodā, tas sastāv no anotācijas (latviešu un angļu valodā), satura, ievada, satura izklāsta sešās pamat nodaļās, secinājumiem un bibliogrāfiskā saraksta. Darba apjoms ir 162 lappuses, tajā iekļauti 161 attēls, 7 tabulas, 113 formulas. Promocijas darba izstrādei izmantoti 53 informācijas avoti.

Contents

INTRODUCTION

Electromagnetic compatibility (EMC) is the branch of electrical sciences which studies the unintentional generation, propagation and reception of electromagnetic energy in conductive form and as radiation, leading to unwanted effects- electromagnetic interference (EMI). EMC ensures the correct operation of electronic equipment in electromagnetic environment. Alternatively, it can be defined as- EMC is the control of EMI. Besides, understanding the phenomena by itself, EMC also addresses the countermeasures, such as control regimes, design and measurements, which should be taken into account to prevent malfunctioning of electronic equipment [1].

Nowadays, electronics is integrated in a wide band of products available in market. Electronics clock speeds are still increasing, leading to low pulse rise-times and fall-times. Electronic components are shrinking in weight and volume, thus leading to compact and lightweight electronic devices. Compact placement of electronic components leads to interaction between them.

The usage of EMI power line filter is one of possibilities to limit conductive noise propagation in the environment. Also, filters are shrinking in size and weight following the electronics evolution. It leads to closely spaced inductors and capacitors that interact to each other, reducing filter performance. Mutual inductance and parasitic capacitance between filter components and PCB becomes a very important aspect in high quality filter design.

This PhD thesis discusses such aspects of EMC filters high frequency parasitic parameters as- three phase power filter parasitic parameter indirect measurement and extraction, 3D electromagnetic field modeling of filter component mutual couplings, filter inductive and capacitive component measurement techniques and measurement errors. PhD thesis describes novel three phase filter parasitic parameter extraction methodology. Three novel EMI power filter capacitor models for 3D electromagnetic field modeling are presented. EMI filter inductive component analysis is carried out using 3D electromagnetic field modeling. Mutual coupling reduction techniques in EMI power filters are developed and analyzed based on 3D electromagnetic field modeling. All modeling results are verified carrying out prototype measurements.

Each chapter is based on at least one scientific publication in an international journal or in an international conference proceeding, therefore thesis is approbated by six scientific publications.

1. EMC PROBLEM ANALYSIS

Electromagnetic compatibility is ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to other equipment, system or services in that environment. Electromagnetic compatibility is an interaction of electrical and electronic equipment with electromagnetic environment and with other equipment, or electromagnetic environment interaction with electrical and electronic equipment.

Equipment and system is electromagnetically compatible with its environment and other equipment and systems, if it satisfies the following three criteria:

1. It does not cause interference with other equipment and systems;
2. It is not susceptible to emissions from other equipment, systems and environment;
3. It does not cause interference with itself.

Designing electromagnetic compatibility is not only important for the desired functional performance. Equipment and systems must also meet legal requirements before they can be offered in the market. There are no harmonized electromagnetic requirements all over the world. Requirements usually vary from country to country. Although, there are countries which agreed to harmonize the requirements to enable the free movement of goods, without country to country specific requirements. As an example European Union can be mentioned; it has developed harmonized electromagnetic compatibility standards and issued Electromagnetic compatibility directive that should be adopted in all member states [2].

Basically, electromagnetic compatibility is concerned with the generation, transmission and reception of electromagnetic energy. These three aspects are illustrated in Fig. 1.1. Source generates the emission and a transfer or coupling path transfers the emission energy to a receptor, where it is resulting in either desired or undesired behavior. Electromagnetic interference (EMI) occurs if the received energy causes the receptor to behave in an undesired manner.

Transfer of electromagnetic energy occurs via couple of paths. Usually these paths are unintentional and electronic engineers are unaware of them. Paths represented in Fig. 1.1. can be observed as paths between two devices or systems as well as paths between components on PCB.

These paths are:

1) Conductive coupling;
2) Inductive coupling;
3) Capacitive coupling;
4) Electromagnetic coupling.

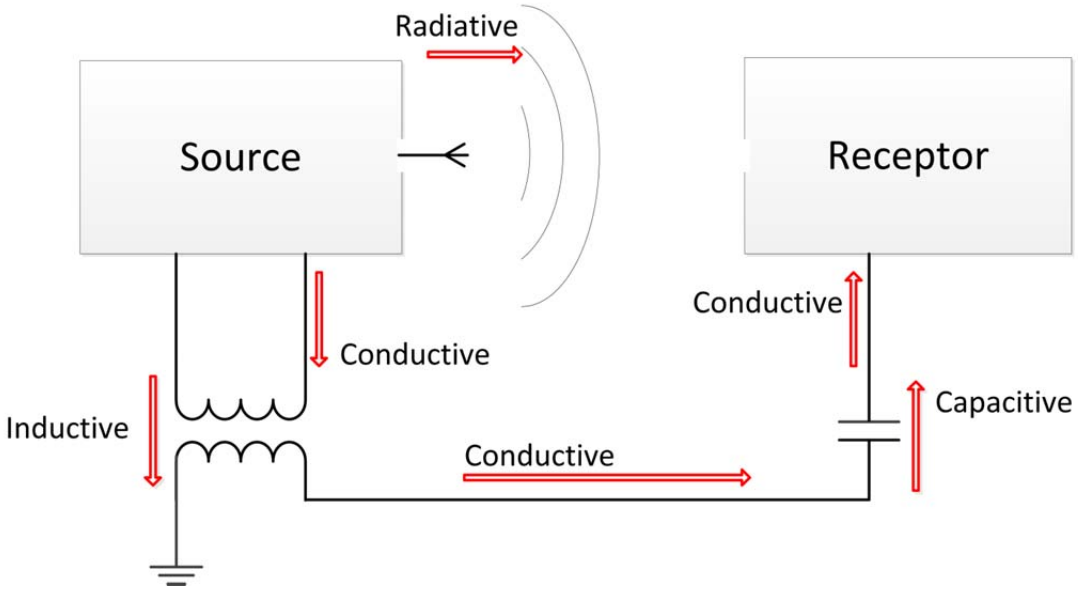


Fig. 1.1. Three aspects of electromagnetic compatibility- source, path, receptor

Conductive coupling happens when the coupling path between the source and the receptor is formed by direct contact with a conducting body. Conducting body can be formed out of transmission lines, PCB trace, wires, cables, heat sinks or enclosures. Inductive coupling happens when a varying magnetic field exists between two conductors in a close distance, inducing a current in nearby conductor. Capacitive coupling happens when a varying electrical field exists between two adjacent conductors in a close distance, inducing a change across the gap between these two conductors. Electromagnetic coupling happens when source and receptor are separated by a large distance, source emits electromagnetic energy and receptor receives electromagnetic energy in terms of electromagnetic waves. It should be noted that "close distance" in EMC usually is defined as distance where magnetic field is dominant and field strength varies as $1/r^3$, $1/r^2$, where r is distance from radiation source. "Large distance" is a distance in which the field strength varies as $1/r^2$ and wave impedance depends on medium it is propagating through (e.g. 377 Ω in vacuum) [3].

To prevent electromagnetic interference three options exist:

1) Decrease emissions at the source;

2) Decrease coupling path efficiency;
3) Increase receptor susceptibility.

The most efficient and economical way to reduce electromagnetic interference is to decrease the emissions at the source. This requires highly qualified engineers to modify the circuits to decrease emissions, but still provide the necessary functions. Receptor susceptibility improvement also requires highly qualified engineers to modify circuits to handle high disturbance impact and still provide its functions. Coupling path efficiency reduction is not as advanced as two tasks mentioned above. There is no need for source and receptor internal circuit management. It is only crucial to know the disturbance propagation path. Various techniques to decrease path efficiency exist, but one technique is common for all paths reduction. It is a filter application. In Fig. 1.2. the application of filters is explained using coupling paths defined in Fig. 1.1.

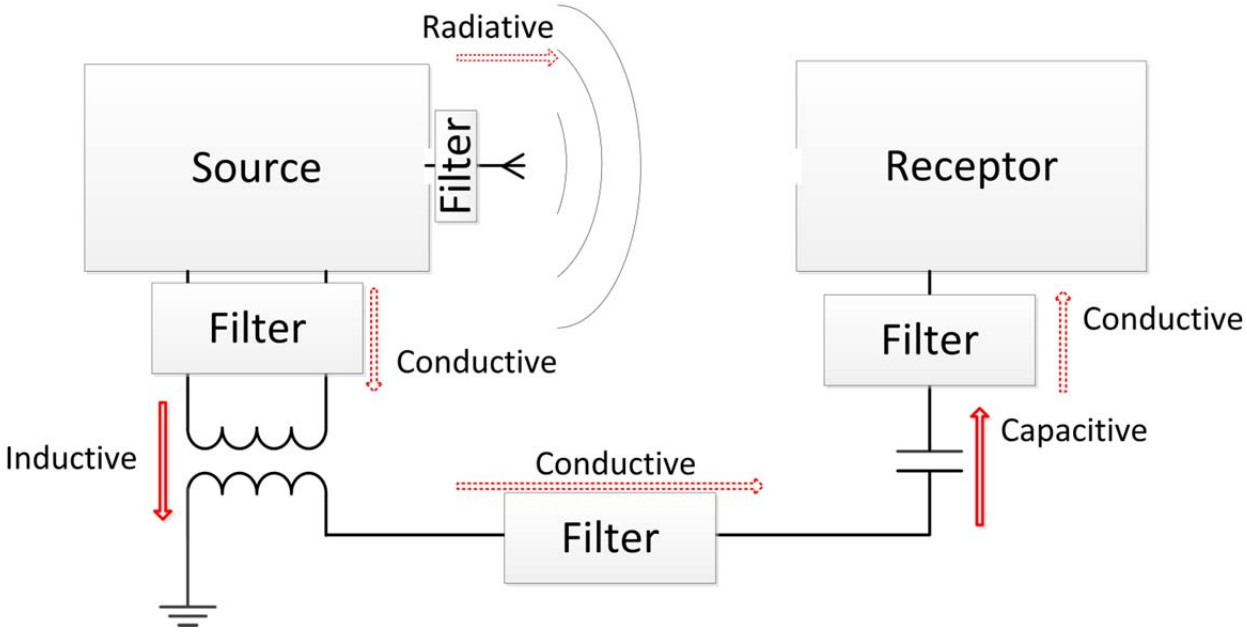


Fig. 1.2. Filter application to reduce coupling paths between source and receptor

Filter installed at the input and output cables of devices and systems reduce the conducted disturbance path efficiency. If the filter is installed in the right position and correctly wired, conductive disturbance reduction will lead also to inductive and capacitive noise reduction. Therefore, elimination of one disturbance path in the right region will lead to electromagnetic interference issue elimination. If the conducted disturbance is reduced at the right region,

electromagnetic disturbances are reduced and there should be no further problems regarding electromagnetic interference.

Since unwanted disturbances usually are at much higher frequencies than useful signals (50Hz mains power, communication signals, sensor signals etc.) filter works by selectively blocking or attenuating unwanted higher frequencies. Basically, the inductive part of the filter is designed to act as a low pass device to enable low frequency useful signal transmission thru the line and attenuating high frequency signal components. Other parts of the filter use capacitors to bypass or shunt unwanted high frequency disturbance. Therefore, passive electromagnetic interference filters are a combination of inductors and capacitors, where each component has its purpose. Unwanted disturbance signal can also appear on antenna terminals, thus feeding unwanted signals to antenna, in combination with useful signals. In his case band pass filters are applicable- filter is designed to pass the useful signal, but attenuate unwanted signal components.

In general EMI problems that must be solved by filter application (or other method usage) are illustrated in Fig. 1.3.:

1) Conducted emissions;
2) Radiated emissions;
3) Conducted susceptibility;
4) Radiated susceptibility.

As this work is focused on filters in frequency range up to couple hundred MHz, in further only conducted emission related EMC problems will be discussed.

There are huge amount of EMC standards that limit the electronic product conducted emissions. These standards can be divided in various groups, depending on environment, product group or specific products. Requirements in these standards differ from product to product, depending on electronic product power, typical usage environment, etc. One of the most widely spread standard is CISPR 11 or its analog EN 55011 “Industrial, scientific and medical equipment– Radio-frequency disturbance characteristics. Limits and methods of measurement.” [4], [5].

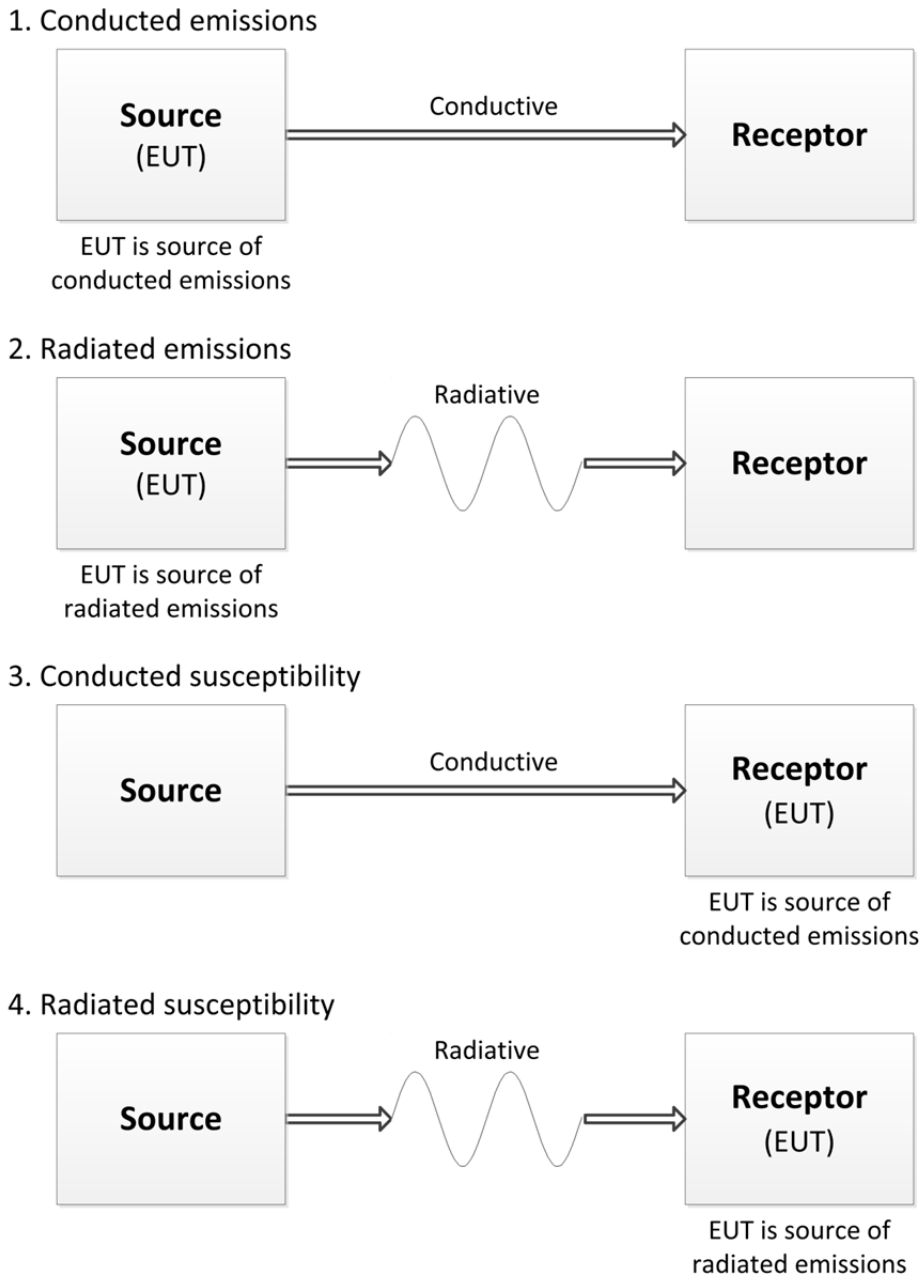


Fig. 1.3. Electromagnetic compatibility emission and susceptibility classification

It defines the conducted emission measurement methodology and defines the conducted emission limits. In Fig. 1.4. EN 55011 conducted emission limit lines are presented for class A and class B equipment.

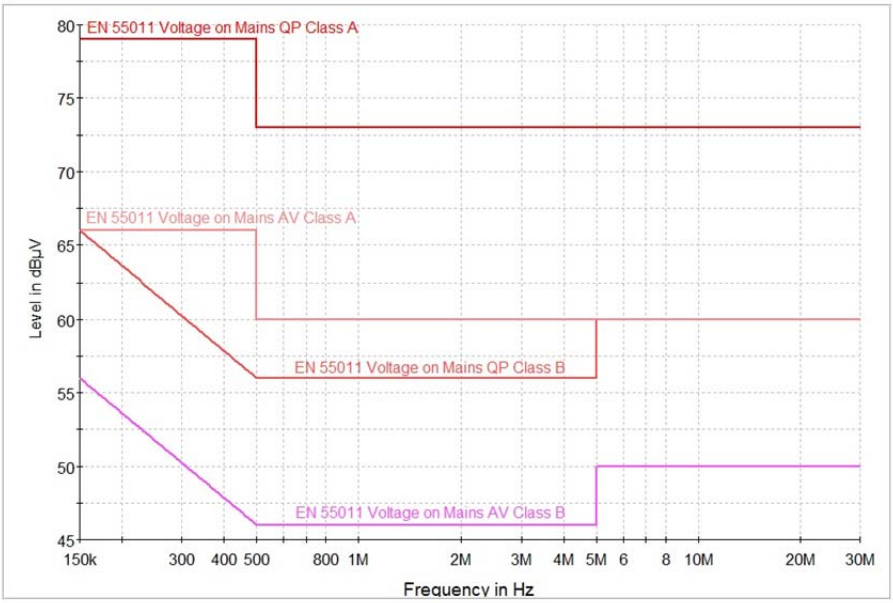


Fig. 1.4. EN 55011 conducted emission limit lines

Conducted emission requirements are defined in range 150kHz- 30MHz. The measurement methodology is defined in Fig. 1.5. Line impedance stabilization network (LISN) is used to measure disturbances created by electronic products or equipment under test (EUT). EUT is connected to the mains network through LISN due to following reasons:

1) LISN defines mains impedance;
2) LISN filters acts as high pass filter and interface to EMI analyzer;
3) LISN acts as filter and attenuates noise coming from mains network.

Fig. 1.5. Conducted emission measurements according to EN 55011

LISN impedance and construction parameters are defined by standards. Simplified LISN schematic is presented in Fig. 1.6. LISN actually is a high pass filter. 50Hz power frequency is

transmitted through LISN power ports without any attenuation from side of mains network, but high frequency components are forwarded to high frequency output (50Hz component is not present at high frequency output). Disturbances from EUT are terminated in defined impedance by the LISN (at 30MHz line-ground impedance is 50Ω) and measured by EMI receiver.

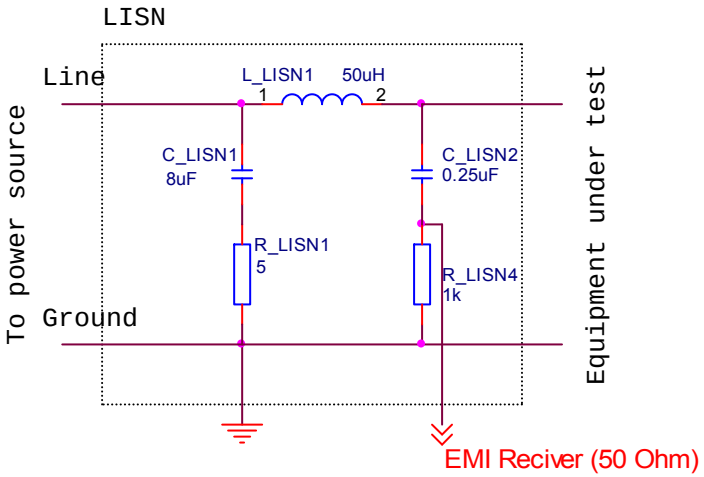


Fig. 1.6. LISN internal circuit

To measure conducted emissions from one phase equipment, it is necessary to have LISN containing combination of two circuits defined in Fig. 1.6., one for line wire and second for neutral wire. For three phase EUT emission measurements there should be LISN with combination of four circuits defined in Fig. 1.6. One phase EUT connected to one phase LISN is shown in Fig. 1.7.

Conducted disturbances are flowing in all wires connected to EUT- line, neutral and grounding. To simplify disturbance analysis disturbances are divided in two groups:

1) Common mode (CM) emissions;
2) Differential mode (DM) emissions.

Differential and common mode currents are shown on simple case in Fig. 1.7. Impedances Z_1 and Z_2 represent the line impedance of EUT and Z_3 represents EUT impedance to ground. Differential mode current i_{DM} flows into line-neutral loop. Common mode current i_{CM} flows in ground wire and creates two loops though line and neutral wires. Therefore, current in each wire separately can be calculated:

$$i_1 = i_{DM} - i_{CM}, \quad (1\text{-}1)$$

$$i_2 = -i_{DM} - i_{CM}, \quad (1\text{-}2)$$

$$i_3 = 2i_{CM}. \tag{1-3}$$

Voltage measured by LISN is (according to EN 55011 Line-Ground and Neutral-Ground impedance is 50Ω):

$$v_1 = 50(i_{DM} - i_{CM}), \tag{1-4}$$

$$v_2 = 50(-i_{DM} - i_{CM}). \tag{1-5}$$

According to equations (1-4) and (1-5), LISN is measuring voltage drop created either by addition or subtraction of common and differential mode currents. To be in compliance with EMC standards these voltage drop values should be lower than limit line defined values.

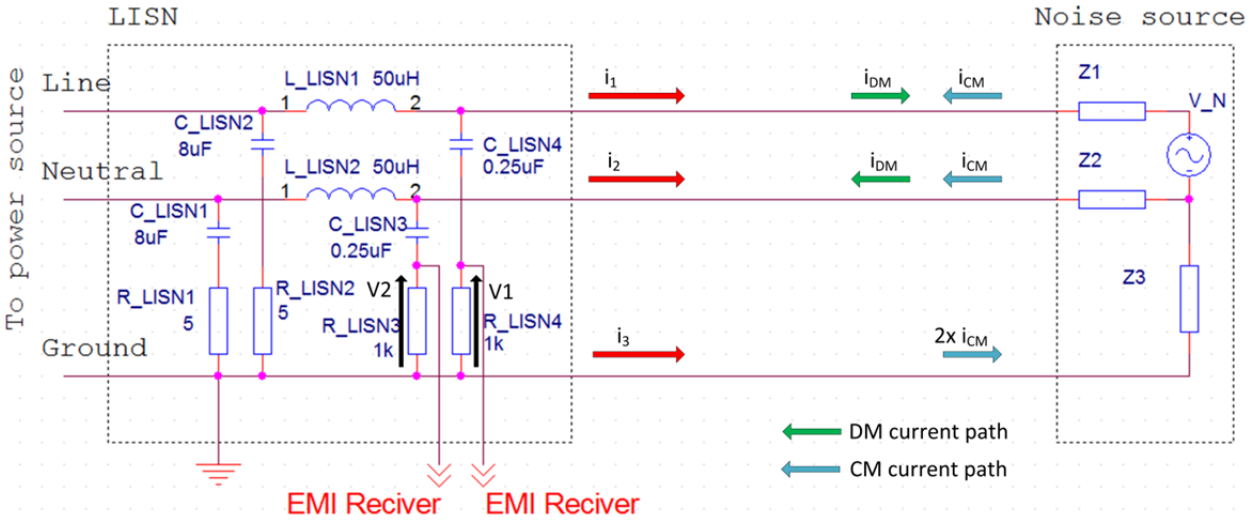


Fig. 1.7. One phase equipment conducted differential mode and common mode emission measurements

The purpose of the EMI filter is to reduce voltage drop V_1 and V_2 to comply with EMC standards. Differential mode and common mode current magnitude depends on disturbance source- EUT. There could be a situation that one of disturbance mode dominates over the other one. Therefore, there is no universal filter circuit that guarantees the compliance with EMC standards. In each situation filter internal circuit should be engineered to effectively reduce disturbance emissions.

The basic principle of components in EMI filter is to bypass disturbance source using shunt capacitors and introduce high impedance to disturbance using series inductors. Filter can be made out of single component- first order filters- such as inductor or capacitor or more advanced topologies creating second, third etc. order filters introducing couple of inductors and

capacitors. Each disturbance mode has its dedicated components and filter topologies, that are used to reduce the current disturbance mode emissions.

Differential mode current is flowing thru two wires (line-neutral in Fig. 1.8.), therefore DM filter is constructed and connected only to these two wires. Basically, DM filter consists of DM inductor and x-capacitor creating LC filters that can be connected in cascades. In Fig. 1.8. DM filter is introduced, containing two LC cascades. Inductor L_2 creates high impedance for high frequency disturbances and capacitor C_{X2} is bypassing it. L_1 and C_{X1} are accomplishing the same task, resulting in decreased voltage measured by LISN- V_1 and V_2. DM filter has no impact on CM disturbance current.

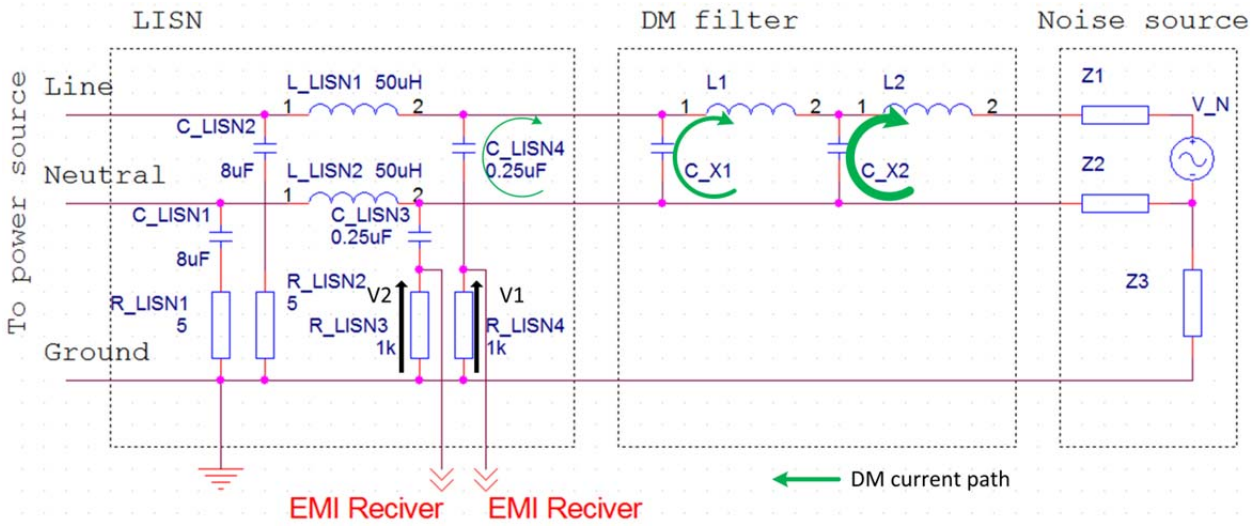


Fig. 1.8. Differential mode filter- two LC cascades

Common mode disturbance current is flowing thru all wires connected to EUT, therefore CM filter should be constructed to reduce current components in all wires. Basically, CM filter is created using CM chokes and y-capacitors. In Fig. 1.9. CM filter two LC cascade topology is introduced. Inductor L2 creates high impedance for high frequency CM current, while capacitors CY3 and CY4 are bypassing the CM current. The same task is accomplished by CM choke L1 and capacitors CY1 and CY2. It should be noted that y-capacitors have impact on DM disturbance current, as CY1, CY2 and CY3, CY4 are connected in series and connected between line and neutral. A possibility to connect inductor in series with ground wire also exists, but this kind of inductor application has drawbacks regarding electrical safety, due to limited ground current capability and raised grounding impedance.

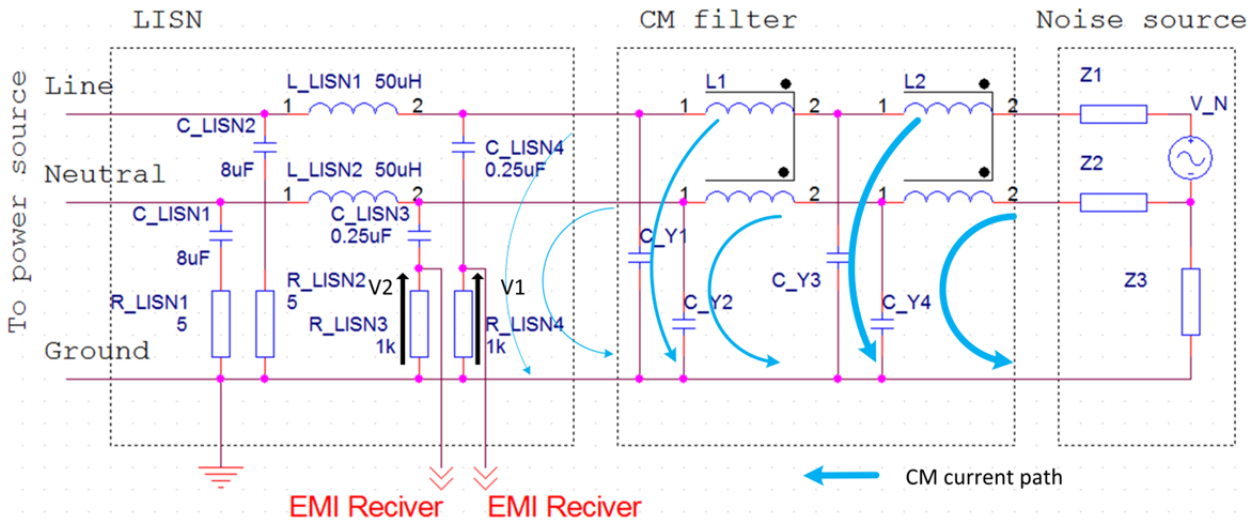


Fig. 1.9. Common mode filter- two LC cascades

To reduce DM and CM disturbances it is necessary to create filter containing both upper mention filter characteristics- DM and CM filtering components. Finally, filter, even for one phase equipment, containing only single stage LC filter for each disturbance mode, consists of at least four components. If disturbance level is higher, the complexity of filter increases.

In high frequencies, filter components- inductors and capacitors, do not perform as ideal components. Component parasitic parameters for capacitors [6], [7], [8] and inductors [9], [10], [11] appear, that degrades filter insertion loss. In literature there are filter component parasitic cancelation techniques presented that can be applied, to improve each component performance, thus improving whole filter performance [6], [12], [13], [14]. Basically, all these cancelation techniques are based on spice type modeling, looking forward for structure optimization. There is no research devoted to industry driven 3D full wave electromagnetic software usage in EMI filter capacitive and inductive component self-parasitic reduction.

Besides, EMI filter component self parasitics, mutual couplings between components exist. To design compact filter, components in filter are placed as close as possible to each other. PCB traces are routed close to each other and close to components. As filter useful filtering bandwidth is pushed up, as more important mutual couplings become. In literature there is couple of publications related to mutual coupling extraction in single phase filters [15], [16]. Mutual coupling measurements are quite complex task, due to the reason that it is impossible to directly measure them. Mutual coupling values should be extracted from array of filter measurements in different configurations. It is very important to know the existing couplings in EMI filters and to know the coupling values, to improve filter performance, despite the time consuming extraction process. High power industrial electronics mainly are based on three phase

power system. But there are no procedures of EMI filter component mutual coupling extraction presented in literature, even not for simple single stage filters.

In power converters at least 30% of its volume is occupied by EMI filter. To further reduce size of the converter care should be taken to design compact EMI filters. If components are mounted next to each other as close as possible, it leads to mutual couplings [17] that lowers filter performance. To design high performance EMI filter, it is necessary to create dozen of prototypes to achieve the desired result, selecting proper components, with desired parasitics, changing PCB layout, changing filter component positions. Modeling can reduce development time. Circuit Spice type modeling in this case is not suitable, as component physical parameters, component relative placement cannot be characterized without additional EMI filter prototype measurements. There have been presented EMI filter modeling techniques [18], [19], [20] that could accelerate development process. But, there is lack of information on techniques using in market available, the most popular 3D electromagnetic modeling tools that could help in more effective manner. However, there are some articles that have described 3D electromagnetic modeling tools in EMI filter modeling [21], [22], [23], but these are not the industry driven 3D electromagnetic modeling tools such as CST Microwave Studio or ANSIS HFSS.

1.1 Conclusions

There is no methodology available for three phase EMI filter component mutual coupling extraction that could give insight in the importance of proper component selection, placement and routing.

Couple of papers regarding conventional EMI filter mutual coupling 3D electromagnetic modeling using dedicated software are available, but there is lack of information on market driven 3D electromagnetic field modeling software usage in EMI filter modeling.

Further chapters will cover upper mentioned aspects. Three phase filter prototype parasitic parameters will be extracted, through array of S-parameter measurements, employing vector network analyzer and Spice based models created, and verified. Novel capacitor models will be developed to enable efficient modeling, using CST Microwave Studio 3D electromagnetic field modeling software. 3D models will be verified using real capacitor measurements. 3D electromagnetic field modeling will be used to model inductive and capacitive EMI power filter components and component interaction- mutual coupling. Modeling tolls will be used to predict mutual coupling reduction techniques to improve filter performance.

All modeling results will be successfully verified using vector network analyzer S-parameter measurements.

2. CHARACTIZATION OF FILTER PARAMETERS USING S-PARAMETERS

2.1 Background

Electromagnetic compatibility (EMC) is mandatory for all electronic devices to access the European Union and other markets. Electronic devices create electromagnetic environment around them self and expose other equipment. Especially industrial and power electronic devices are powerful disturbance sources and their perilous gains due to possibility of portable movement and connection to almost all power supply grids [24]. To comply with one of the emission types- conducted emissions, power line filters are used in nearly all electronic devices. Power line filters are selected to attenuate conducted emission disturbances in defined frequency range, which depends on the disturbance source. Filter attenuation in frequency range is defined as insertion loss. Filters insertion loss is dependent value. It depends on source and load impedances, thus filters performance in real electronic system cannot be predicted, without knowledge of these parameters. Usually insertion loss of filter is measured using 50Ω termination in load and in source. Moreover, an international standard CISPR 17 is published that defines other insertion loss measurement techniques called "Approximate worst case". Despite this method is used for characterization of filters widely, there is a necessity to develop, improve and use characterization method that is independent of noise source and load impedances. Such characterization method is proposed in source [25] and improved in source [26], using two port network characteristic parameters- scattering parameters (S-parameters).

2.2 Conventional characterization of filters

EMI filters are typically characterized by their insertion loss, which is usually stated in decibels (dB). Filter is typically inserted between the source of the disturbances and load, in order to prevent the unwanted disturbance signals to affect the performance of load. The situation is shown in Fig. 2.1.

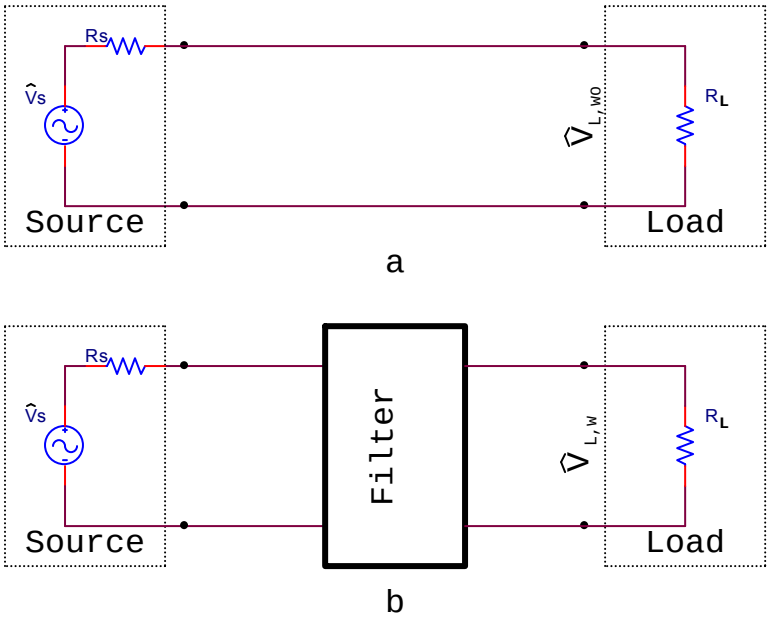


Fig. 2.1. Typical application of power line filter

Load voltage with filter are denoted by $V_{L,w}$, but load voltage without filter are denoted by $V_{L,wo}$. Therefore, the insertion loss is defined by equations (2-1) and (2-2) [27]:

$$IL_{dB} = 10\log_{10}\left(\frac{P_{Lwo}}{P_{Lw}}\right) = 10\log_{10}\left(\frac{\frac{V_{Lwo}^2}{R_L}}{\frac{V_{Lw}^2}{R_L}}\right), \tag{2-1}$$

where IL_{dB}- insertion loss in dB,

P_{Lwo}- power on load without filter,

P_{Lw}- power on load with filter,

P_{Lw}- power on load with filter,

V_{Lwo}- load voltage without filter,

V_{Lw}- load voltage with filter,

R_L- load resistance,

and

$$IL_{dB} = 20\log_{10}\left(\frac{V_{Lwo}}{V_{Lw}}\right). \tag{2-2}$$

Insertion loss reduces the voltage due to the insertion of the filter, at the frequency of interest. Filters specification are often given assuming that the source and load impedances are equal to some specified value (50Ω is usual value). Engineers with years of experience in EMC admit these attenuation curves, generally prepared from data taken in a 50Ω test setup, to be of extremely limited value. In spite of the low benefit of this information, manufactures publish

50Ω data, because of the easy measurement procedures and equipment availability, since connectors, test cables and instrumentation characteristic impedance are 50Ω. Attenuation curves using 50Ω impedance are often criticized in many books and technical papers as well as in insertion loss measurement standards such as Mil Std 220 [28] and CISPR 17 [29]. CISPR 17 proposes an alternative measuring method the so called "Approximate Worst Case Method". This test method uses 0.1Ω and 100Ω terminations on the line and load side, instead of 50Ω termination, measuring the filter insertion loss. Afterwards the measurements are repeated changing the termination impedances 100Ω and 0.1Ω terminations on the line and load side. Although this test method is not the same as measuring a filter in a real equipment installation, the normalized results can be used with relative accuracy to predict the performance of the filter in a real situation. Another advantage of CISPR 17 - measurement method is well defined, that leads to accurate and repeatable results. The power line filter industry must publish data on its products using recognized, standardized and accepted test methods. If, as generally accepted, the 50Ω method cannot be used to predict the performance of a filter in real equipment, the CISPR 17 "Approximate Worst Case" method is the only such standardized test to meet this requirement [30].

To determinate the actual insertion loss in dB, if the source and load impedances are known, equation (2-3) or (2-4) can be used, depending on the filters characteristic transfer impedance. Equation (2-3) is valid in case, if the filter is used as shunt or in parallel with load and source.

$$IL_{dB} = 20\log_{10}\left|1 + \frac{Z_S Z_L}{Z_T(Z_S + Z_L)}\right| \quad , \tag{2-3}$$

where Z_S- source impedance,

Z_L- load impedance,

Z_T- filters impedance,

and

$$IL_{dB} = 20\log_{10}\left|1 + \frac{Z_T}{Z_S + Z_L}\right| \quad . \tag{2-4}$$

The impedance Z_T would be equal to the ratio of the voltage across the open circuited output of the filter, to the current into the filter. Using voltage division and algebra, insertion loss can be obtained as follows:

$$IL_{dB} = 20\log_{10}\left|\frac{\frac{V_{Lwo}}{V_S}}{\frac{V_{Lw}}{V_S}}\right| = 20\log_{10}\left|\frac{\frac{Z_L}{Z_L+Z_S}}{\frac{\frac{Z_L Z_T}{Z_L+Z_T}}{\frac{Z_L Z_T}{Z_L+Z_T}+Z_S}}\right|, \quad (2\text{-}5)$$

where V_S- source voltage.

As an example for shunt filter the capacitor can be mentioned. Thus, capacitor impedance should be modeled as RLC circuit representing real capacitor in applicable frequency range.

Equation (2-4) is valid in case if the filter is used in series with load source. Filters insertion loss can easily be obtained with equation (2-6):

$$IL_{dB} = 20\log_{10}\left|\frac{\frac{V_{Lwo}}{V_S}}{\frac{V_{Lw}}{V_S}}\right| = 20\log_{10}\left|\frac{\frac{Z_L}{Z_L+Z_S}}{\frac{Z_L Z_T}{Z_L+Z_T+Z_S}}\right| = 20\log_{10}\left|1+\frac{Z_T}{Z_S+Z_L}\right|. \quad (2\text{-}6)$$

Filters used in series for power electronic are ferrite chokes and beads.

2.3 EMI filters characterization using scattering parameters

EMI filter can be represented as two port network. In case of three phase filters, filter can be divided in separate three phases and characterized phase by phase as simple one phase filter. A two-port network gives the possibility to isolate complete circuit (filter) out of a complete system replacing it by its characteristic parameters. Once this is done, the characterized part of the system- filter- becomes a "black box" with a set of distinctive properties, enabling simple analysis of it. There are a number of alternative sets of parameters that can be used to describe a linear two-port network. The usual sets are, respectively, called Z, Y, H, G, and ABCD parameters. These are all limited to linear networks since an underlying assumption of their derivation is that any given circuit condition is a linear superposition of various short-circuit and open circuit conditions. Z, Y, H, G, and ABCD parameters measurement requires either a short or an open circuit measurement at each of the ports that is difficult task in high frequency range, due to parasitic parameters of an open circuit and a short circuit. Moving to higher and higher frequencies, such problems arise: equipment is not readily available to measure total voltage and total current at the ports of the network, short and open circuits are difficult to achieve over a broad band of frequencies.

S-parameters (Scattering parameters) differ from *Z*, *Y*, *H*, *G*, and *ABCD* parameters, in the sense that S-parameters do not use open or short circuit conditions to characterize a linear electrical network. Instead, matched loads are used. These terminations are much easier to use at high signal frequencies than an open-circuit and a short-circuit terminations. The quantities are measured in terms of power. In the context of S-parameters, scattering refers to the way how the traveling currents and voltages in a transmission line are affected when they meet a discontinuity caused by the insertion of a network into the transmission line. Measuring the filter, long connecting cables and connections are used, that introduces such parasitic parameters as parasitic capacitance and inductance, for S-parameters they are calibrated for two filter ports, so parasitic capacitance and inductance effect are excluded from measurement results. Consequently measurement results are more accurate especially in high frequency, in comparison to *Z*, *Y*, *H*, *G*, and *ABCD* parameter measurement.

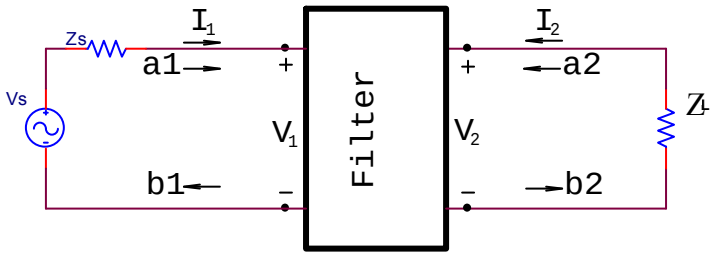


Fig. 2.2. Two port network- EMI filter, where

a1, a2- incident waves on source side and load side;

b1, b2- reflected waves on source side and load side;

I1, I2- input current at port 1 and port 2;

V_1, V_2- input voltage at port 1 and port 2;

V_S- voltage source;

Z_s- source impedance;

Z_L- load impedance.

In Fig. 2.2. EMI filter is represented as two port network, connected to source and load and analyzed in terms of waves. It is reasonable to characterize an EMI filter as linear passive two port network under small signal excitation conditions. Although EMI filter consists of nonlinear components, such as inductors, they can be assumed to be linear under small signal excitation. Non linearity effect can be measured and modeled using current biases superimposed during the small signal excitation measurements.

Generalized scattering parameters have been defined by K. Kurokawa [31]. These parameters describe the interrelationships of variables a_1, a_2, b_1 and b_2. These variables are

normalized complex voltage waves incident on and reflected from the port1 and port2 of the network. They are defined in terms of terminal voltage V_1, V_2 and terminal current I_1,I_2, and an arbitrary reference impedance Z_0, respectively, all variables and parameters will be referenced to a single positive real impedance, Z_0=50Ω. Voltage and current are stated in RMS values. The independent variables a_1 and a_2 are normalized incident waves, as stated in equations (2-7) and (2-8):

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}}, \tag{2-7}$$

where a_1- normalized incident wave on port1,

V_1- voltage on port1,

I_1- current on port1,

Z_0- reference impedance,

V_{i1}- incident voltage on port1 .

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}}, \tag{2-8}$$

where a_2- is normalized incident wave on port2,

V_2- voltage on port2,

I_2- current on port2,

V_{i2}- incident voltage on port2.

Dependent variables b_1 and b_2, are normalized reflected voltages as stated in equations (2-9) and (2-10):

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}}, \tag{2-9}$$

where b_1- is normalized reflected wave from port1,

V_{r1}- voltage wave reflected from port1.

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}}, \tag{2-10}$$

where b_2- is normalized reflected wave from port2,

V_{r2}- voltage wave reflected from port2.

Or in terms of incident waves and reflected waves port voltages and currents can be expressed using equations (2-11) - (2-14):

$$V_1 = \sqrt{Z_0}(a_1 + b_1), \tag{2-11}$$

$$V_2 = \sqrt{Z_0}(a_2 + b_2)\,, \tag{2-12}$$

$$I_1 = \frac{1}{\sqrt{Z_0}}(a_1 - b_1)\,, \tag{2-13}$$

$$I_2 = \frac{1}{\sqrt{Z_0}}(a_2 - b_2)\,. \tag{2-14}$$

Network displayed in Fig. 2.2., using incident and reflected waves can be fully characterized, using two linear equation system (2-15) or in form of matrices (2-16).

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases}, \tag{2-15}$$

where S_{11}- is input reflection coefficient,

S_{12}- forward transmission coefficient,

S_{21}- reverse transmission coefficient,

S_{22}- output reflection coefficient.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}\,. \tag{2-16}$$

When incident wave a_1 or a_2 reaches the two port network, because of the impedance mismatch, the wave is reflected creating reflected wave b_1 or b_2. Also reflected waves b1, b2 reaching source and load are reflected because of the impedance mismatch. In transmission line theory these effects are described using reflection coefficients:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}\,, \tag{2-17}$$

where Γ_L- is load reflection coefficient,

Z_L- load impedance.

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}\,, \tag{2-18}$$

where Γ_S- is source reflection coefficient,

Z_S- source impedance.

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\,, \tag{2-19}$$

where Γ_{in}- is input reflection coefficient of two port network,

Z_{in}- filter input impedance.

$$\Gamma_{out} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\,, \tag{2-20}$$

where, Γ_{out}- is output reflection coefficient of two port network,

Z_{out}- filter output impedance.

Using signal flow graphs, circuit in Fig. 2.2. can be characterized in different way- Fig. 2.3. Flow graph usage simplifies network analysis, due to, 'non touching loop rule' or Mason's gain formula that is a method for finding the transfer function of a linear signal-flow graph. Normalized wave emanating from source are defined as b_s for defined source voltage V_S and source impedance Z_S:

$$b_S = \frac{\sqrt{Z_0}V_S}{Z_S + Z_0}\,, \tag{2-21}$$

where b_S- normalized wave emanating from source.

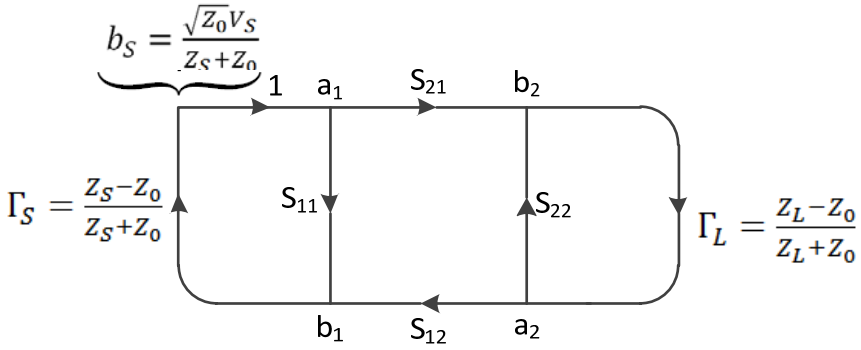


Fig. 2.3. Flow graph of the two port network circuit

Using Manson's gain formula to find the transfer function of a linear signal-flow graph shown in Fig. 2.3., it is possible to define following relations:

$$\frac{a_2}{b_S} = \frac{S_{21}\Gamma_L}{1-(S_{11}\Gamma_S + S_{21}\Gamma_L S_{12}\Gamma_S + S_{22}\Gamma_L) + S_{11}\Gamma_S S_{22}\Gamma_L}\,, \tag{2-22}$$

$$\frac{b_2}{b_S} = \frac{S_{21}}{1-(S_{11}\Gamma_S + S_{21}\Gamma_L S_{12}\Gamma_S + S_{22}\Gamma_L) + S_{11}\Gamma_S S_{22}\Gamma_L}\,, \tag{2-23}$$

$$\frac{a_1}{b_S} = \frac{(1-S_{22}\Gamma_L)}{1-(S_{11}\Gamma_S + S_{21}\Gamma_L S_{12}\Gamma_S + S_{22}\Gamma_L) + S_{11}\Gamma_S S_{22}\Gamma_L}\,, \tag{2-24}$$

$$\frac{b_1}{b_S} = \frac{S_{11}(1-S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}}{1-(S_{11}\Gamma_S + S_{21}\Gamma_L S_{12}\Gamma_S + S_{22}\Gamma_L) + S_{11}\Gamma_S S_{22}\Gamma_L}\,. \tag{2-25}$$

In microwave theory input to output voltage gain is defined in term of S-parametrs and reflection coefficients as in equation (2-26). Therefore input to output voltage gain is defined differently, as stated in EMI filters design theory [32]. Input and output voltages are measured with the inserted filter between the source and load, as in Fig. 2.2.

$$A_v = \frac{V_2}{V_1} = \frac{S_{21}(1+\Gamma_L)}{(1-S_{22}\Gamma_L)(1+S_{11}')}\,, \tag{2-26}$$

where $S_{11}^{'} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$ – input reflection coefficient with arbitrary load impedance.

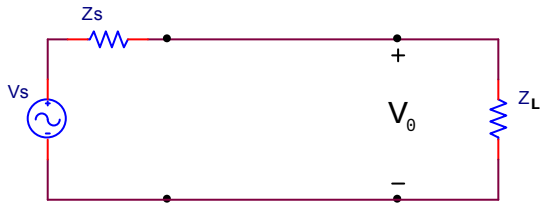


Fig. 2.4. Circuit to define insertion loss- insertion voltage gain

In EMI filter design theory [33] insertion voltage gain or insertion loss is defined as ratio of voltage at load without filter and voltage at load with filter. So, equation (2-26) cannot be used in EMI filter insertion loss calculation. According to [26] it is possible to develop equation satisfying EMI filter theory using S-parameters and reflection coefficients. Insertion voltage gain of an EMI filter according to EMI filters theory satisfies equation (2-27).

$$A_V = \frac{V_2}{V_0} = \frac{V_2}{\frac{Z_L}{Z_S+Z_L}V_S} = \frac{V_2}{\frac{Z_L}{Z_S+Z_L}(V_1+I_1Z_S)}, \tag{2-27}$$

where V_2, V_1, I_1- voltages defined in Fig. 2.2,

I_1- current defined in Fig. 2.2,

V_0, V_S- voltages defined in Fig. 2.4,

Z_L, Z_S- load and source impedances equal in both Fig. 2.2. and Fig. 2.4.

Equation (2-27) can be modified using substitution with equations (2-11),(2-12) and (2-13):

$$A_V = \frac{\frac{a_2}{b_S}+\frac{b_2}{b_S}}{\frac{a_1}{b_S}\left(1+\frac{Z_S}{Z_0}\right)+\frac{b_1}{b_S}\left(1-\frac{Z_S}{Z_0}\right)}\left(\frac{Z_S+Z_L}{Z_L}\right). \tag{2-28}$$

Using equations (2-22) – (2-25) and (2-17), (2-18) it is possible to develop insertion voltage gain in terms of reflection coefficients and scattering parameters according to EMI filters design theory [26]:

$$A_V = \frac{S_{21}(1-\Gamma_L\Gamma_S)}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{21}\Gamma_L S_{12}\Gamma_S}. \tag{2-29}$$

Insertion voltage gain can be calculated using direct measurement of S_{11}, S_{12}, S_{21}, S_{22} with vector network, vector analyzer and calculation of reflection coefficients using equations (2-17) and (2-18). Reflection coefficients are calculated using- Z_L, that is defined by LISN (for DM filter LISN impedance is 100Ω, for CM filter LISN impedance is 25Ω), Z_0=50Ω and Z_S, that is source impedance, obtained as in [34], [35].

Consequently, A_V or voltage insertion gain of filter is affected by source and load impedances Z_S, Z_L via reflection coefficients Γ_S, Γ_L, but the filter is characterized only by scattering parameters S_{11}, S_{12}, S_{21}, S_{22} independent of Z_S and Z_L. Due to the calibration it is possible to measure them directly on ports of EMI filter and no open or short circuit is needed, the measurements are expected to be more accurate in high frequency region than [Z], [Y], [H] and [ABCD] network parameter measurements.

It should be noted that S_{21}- reverse transmission coefficient, is also called voltage insertion gain, when Z_S and Z_L are equal to network characteristic impedance- Z_0. If $Z_S = 50\Omega;\ Z_L = 50\Omega$, then $\Gamma_S = 0, \Gamma_L = 0$, thus equation (2-29) simplifies:

$$A_V = \frac{S_{21}(1 - \Gamma_L\Gamma_S)}{(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{21}\Gamma_L S_{12}\Gamma_S} = S_{21}\ . \tag{2-30}$$

2.4 Filter design according to waves theory

Scattering parameters are characterizing the filter independently of the source and load impedances. But filters response in a real system is still dependent on source and load impedance and these should be taken into account in filter design. Filter input and output reflection coefficients are parameters that can be used to design filter, from standpoint of waves [26]. According to Manson's gain formula reflected wave b_1 in Fig. 2.3. can be expressed as follows:

$$b_1 = a_1\left(S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L}\right). \tag{2-31}$$

Load impedance of EMI filter is known value- LISN impedance for CM is 25Ω and for DM 100Ω. Thus the load reflections are:

$$DM\colon \Gamma_L = \frac{1}{3}\ and\ CM\colon \Gamma_L = -\frac{1}{3}\ . \tag{2-32}$$

EMI filter forward and reverse transmission coefficients S_{21} and S_{12} are much smaller than reflection coefficients S_{11} and S_{22}, in addition $0 \le |S_{22}| \le 1$ and $0 \le |S_{11}| \le 1$, therefore equation (2-31) can be simplified:

$$b_1 \approx a_1 S_{11}\ . \tag{2-33}$$

According to equation (2-33) in Fig. 2.3 showed signal flow graph can be simplified as shown in Fig. 2.5.

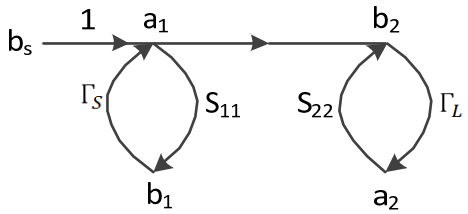


Fig. 2.5. Simplified EMI filter flow graph

Further equation (2-29) can be simplified as follows:

$$|A_V| \approx \frac{|S_{21}||1-\Gamma_L\Gamma_S|}{|1-S_{11}\Gamma_S||1-S_{22}\Gamma_L|} \ . \tag{2-34}$$

Taking in to account equation (2-34) it is obvious that S_{21} should be reduced to maximize insertion voltage gain and denominator fractions- $|1-S_{11}\Gamma_S|$ and $|1-S_{22}\Gamma_L|$ should be kept as large as possible. Since reflection coefficients Γ_L and Γ_S are from filter independent parameters, filter designer can design filter with custom S_{11} and S_{22} parameters to enlarge voltage insertion gain.

2.4.1 DM filter design according to waves theory

Three phase frequency converter consisting of rectifier and capacitor input reflection coefficient leads to Γ_S=-1, doe to small capacitor impedance. Therefore, to maximize the product of $|1-S_{11}\Gamma_S|$, S_{11} should approach 1, consequently, a high filter input impedance should be designed. In case of three phase active harmonic filters with large inductors at the input, reflection coefficient leads to Γ_S=1. Therefore to maximize the product of $|1-S_{11}\Gamma_S|$, S_{11} should approach -1, consequently, a low filter input impedance should be designed. LISN is connected to the filter load side, thus $\Gamma_L = \frac{1}{3}$. Therefore, to maximize $|1-S_{22}\Gamma_L|$, S_{22} should approach -1, consequently, a low filter impedance should be designed at the load side.

2.4.2 CM filter design according to waves theory

In case of CM filter, the source impedance is created by small parasitic capacitances in electronic equipment, thus leading to high impedance, therefore reflection coefficient leads to Γ_S=1. To maximize the product of $|1-S_{11}\Gamma_S|$, S_{11} should approach -1, consequently, a low filter input impedance should be designed. LISN is connected to the filter load side, thus

$\Gamma_L = -\frac{1}{3}$. To maximize $|1 - S_{22}\Gamma_L|$, S_{22} should approach 1, consequently, a high filter impedance should be designed at the load side.

To obtain high or low impedance at filter input and output ports, capacitors and inductors are used. Capacitors are used in parallel with filter ports to obtain low impedance. Inductors are used in series with ports to obtain high impedance.

Impedance mismatch rule used in conventional EMI filter design is the same as filter input and output impedance requirement from standpoint of reflected waves.

2.5 Scattering parameter relationships

In the same manner as S-parameters are defined, it is possible to define network impedance parameters Z-parameters. Two port T-network represented in Fig. 2.6., can be described with Z-parameters in case of open circuit, using equations (2-25) and (2-26).

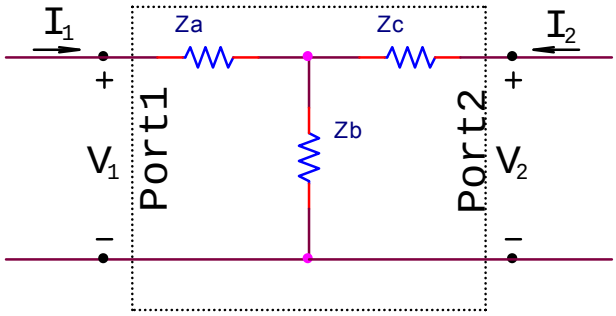


Fig. 2.6. Two port T-network

$$Z_{11} = Z_a + Z_b \text{ if } I_2 = 0\,, \tag{2-35}$$

where Z_{11}, Z_a, Z_b- two port network parameters, according to Fig. 2.6.,

I_2- two port network port2 current, according to Fig. 2.6.

$$Z_{22} = Z_c + Z_b \text{ if } I_1 = 0\,, \tag{2-36}$$

where Z_{22}, Z_c, - two port network parameters, according to Fig. 2.6.,

I_1- two port network port1 current, according to Fig. 2.6.

If input current is I_1, the open circuit output voltage is I_1Z_b, so $Z_{12} = Z_b$. Solving equations (2-35) and (2-36) for Z_a, Z_b and Z_c it can be stated:

$$Z_{11} - Z_{12} = Z_a\,, \tag{2-37}$$

where Z_{12}- two port network parameter, according to Fig. 2.6.

$$Z_{22} - Z_{12} = Z_c \ , \tag{2-38}$$

$$Z_{12} = Z_{21} = Z_b \ , \tag{2-39}$$

where Z_{21}- two port network parameter, according to Fig. 2.6.

Two port network Z-parameters similarly as S-parameters are described by as follows:

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \ , \tag{2-40}$$

where V_1- two port network port1 voltage, according to Fig. 2.6.

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \ , \tag{2-41}$$

where V_2- two port network port2 voltage, according to Fig. 2.6.

As long as network parameters are measured in terms of S-parameters it is useful to convert them in terms of Z-parameters, if it is necessary to analyze two port network as T-network, where S-parameters are normalized to reference impedance Z_0 [36]. Then

$$Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \ , \tag{2-42}$$

$$Z_{12} = \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \ , \tag{2-43}$$

$$Z_{21} = \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \ , \tag{2-44}$$

$$Z_{22} = \frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \ . \tag{2-45}$$

Inserting equations (2-42), (2-43), (2-44) and (2-45) into equations (2-37), (2-38) and (2-39), expressions, characterizing separate two port T-network impedances- Za, Zb, Zc, can be derived, thus they are normalized to characteristic impedance Z_0:

$$Z_a = Z_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{21}^2 - 2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{21}^2} \ , \tag{2-46}$$

$$Z_b = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{21}^2} \ , \tag{2-47}$$

$$Z_c = Z_0 \frac{(1 + S_{22})(1 - S_{11}) + S_{21}^2 - 2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{21}^2} \ . \tag{2-48}$$

Equations (2-46), (2-47) and (2-48) are used in next chapters in extraction of mutual inductances. In Fig. 2.7a filter consisting of capacitors C1 and C2, with parasitic parameters ESL1, ESL2 and ESR1, ESR2 and mutual inductance M3, are represented. The same filter circuit with decoupled inductances is represented in Fig. 2.7b. Assuming that filter represents two port T- network, carrying out S-parameter measurements it is possible to calculate directly mutual inductance impedance between capacitors- Z_b.

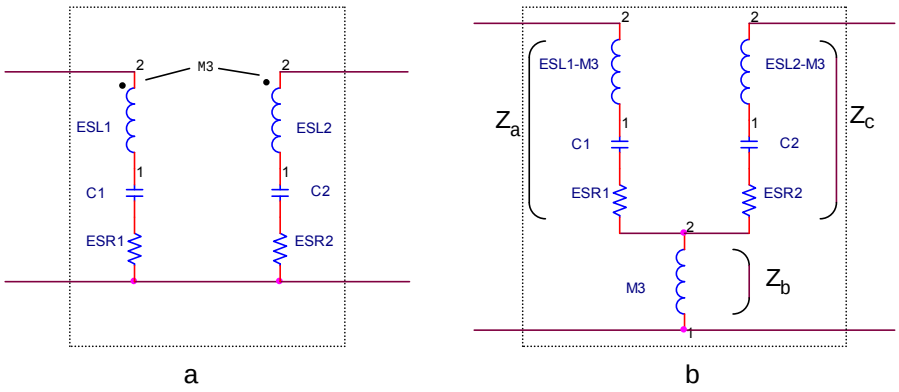


Fig. 2.7.(a) Two port T-network (b) Decoupled two port T-network

The proposed method [26] has been successfully used for one phase filter mutual parameter extraction, in this work this method first time will be used for the three phase filter parasitic parameter extraction.

2.6 Filter capacitor impedance measurements using scattering parameters

S-parameter measurements can be used also in filter component characterization. Capacitors and inductors can be described with lumped element models that simplify the description of the behavior of spatially distributed physical systems into a topology consisting of discrete entities that approximate the behavior of the distributed systems under certain assumptions. In Fig. 2.8. capacitor and inductor lumped element models are shown, as two port networks. There is a couple of models for each component, suitable for different situation. In Fig. 2.8. lumped element models are only examples for measurement methodology and error analysis.

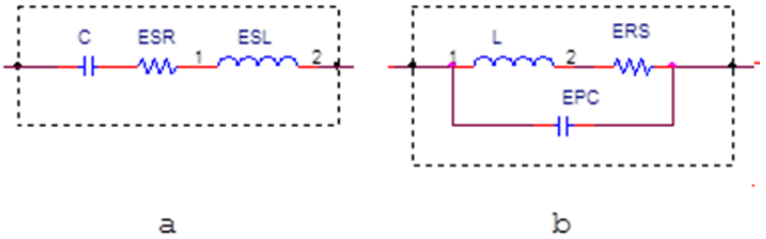


Fig. 2.8. a) Capacitor lumped element model, b) Inductor lumped element model

If components are treated as two port networks it is enough to measure impedance Z_{11}, that gives enough data to calculate C, ESL, ESR for capacitors and L, ESR, EPS for inductors. There are

three impedance Z_{11} measurement methods for two port networks that utilize vector network analyzer, Fig. 2.9. Therefore, it is important to analyze them and to choose the proper one to obtain the results with highest precision.

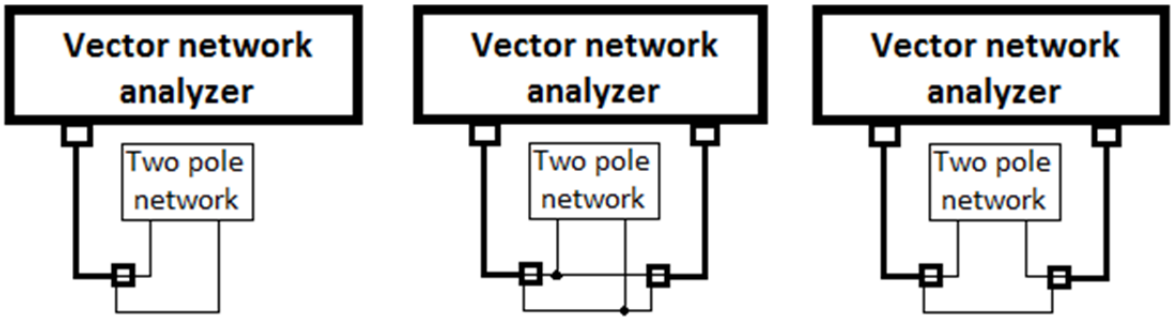
Three methods for Z_{11} measurement [37]:

1. Reflection coefficient- S_{11}, measurement using one vector network analyzer port, if two port network is connected in parallel to the vector network analyzer port;
2. Reverse transmission coefficient- S_{21}, measurement if two port network is connected in parallel with the vector network analyzer ports;
3. Reverse transmission coefficient- S_{21}, measurement if two port network is connected in series with the vector network analyzer ports.

Impedance Z_{11} measurement error is high, if measured $|S_{11}|$ or $|S_{21}|$ is close to 0dB or 1. Therefore, the selection of measurement method depends on the impedance $|Z_{11}|$:

1. The first method is recommendable if $|Z_{11}|$ is close to 50Ω, as in this case $|S_{11}|$ will be much lower than 0dB;
2. The second method is recommendable if $|Z_{21}|$ is lower than 10Ω, as in this case $|S_{21}|$ will be much lower than 0dB;
3. The third method is recommendable if $|Z_{21}|$ is higher than 100Ω, as in this case $|S_{21}|$ will be much lower than 0dB.

In case of EMI filter capacitor measurements in frequency range up to few tens of MHz, it is recommended to use the second method, as capacitors impedance in this frequency range usually is lower than 10Ω.



a) b) c)

Fig. 2.9. Three impedance measurement techniques using vector network analyzer: a) first method, b) second method, c) third method

Using first impedance Z_{11} measurement method, which employs only one vector network analyzer port, S_{11} parameter is measured, that gives a possibility to calculate Z_{11}:

$$Z_{11} = 50\frac{1+S_{11}}{1-S_{11}} = 50\frac{1-|S_{11}|^2 + j2|S_{11}|\sin\varphi}{1-2|S_{11}|\cos\varphi+|S_{11}|^2}, \quad (2\text{-}49)$$

where φ- S11 reflection coefficient phase.

Real part of Z11 impedance can be calculated using (2-50) as follows:

$$\mathrm{Re}\{Z_{11}\} = 50\frac{1-|S_{11}|^2}{1-2|S_{11}|\cos\varphi+|S_{11}|^2}. \quad (2\text{-}50)$$

Therefore, imaginary part can be calculated using (2-51) as follows:

$$Im\{Z_{11}\} = 100\frac{|S_{11}|\sin\varphi}{1-2|S_{11}|\cos\varphi+|S_{11}|^2}. \quad (2\text{-}51)$$

Modulus of impedance Z11:

$$|Z_{11}| = \sqrt{(\mathrm{Re}\{Z_{11}\})^2 + (\mathrm{Im}\{Z_{11}\})^2} = \frac{50}{1-2|S_{11}|\cos\varphi+|S_{11}|^2}\sqrt{\left(1-|S_{11}|^2\right)^2 + \left(100|S_{11}|\sin\varphi\right)^2}. \quad (2\text{-}52)$$

In case if measured two-pole network $|Z_{11}|$ is much lower than 50Ω, then $|S_{11}|$ will be close to 1 or 0dB and two-pole network impedance $|Z_{11}|$ error can reach 100%. It should be noted that real part of $|Z_{11}|$ represents the capacitor equivalent series resistance- ESR. As the error of impedance $|Z_{11}|$ can reach 100%, it is not recommended to use first method, Fig. 2.9.a, in EMI filter capacitor measurements.

Using second measurement method represented in Fig. 2.9.b, where two-pole network is connected in parallel to both ports of vector network analyzer, impedance Z_{11} can be calculated using, (2-55) [38]:

$$Z_{11} = 25\frac{S_{21}}{1-S_{21}} = 25\frac{|S_{21}|\cos\varphi - |S_{21}|^2 + j|S_{21}|\sin\varphi}{1-2|S_{21}|\cos\varphi + |S_{21}|^2}. \tag{2-53}$$

Real part of impedance can be calculated using:

$$\mathrm{Re}\{Z_{11}\} = 25\frac{|S_{21}|\cos\varphi - |S_{21}|^2}{1-2|S_{21}|\cos\varphi + |S_{21}|^2}. \tag{2-54}$$

Therefore, imaginary part can be calculated using:

$$Im\{Z_{11}\} = 25\frac{|S_{21}|\sin\varphi}{1-2|S_{21}|\cos\varphi + |S_{21}|^2}. \tag{2-55}$$

Modulus of impedance Z_{11} can be calculated:

$$|Z_{11}| = \frac{25|S_{21}|}{\sqrt{1-2|S_{21}|\cos\varphi + |S_{21}|^2}}. \tag{2-56}$$

If $|Z_{11}| \ll 50\Omega$ ($|S_{21}| \ll 1$), then (2-53) can be rewritten as:

$$Z_{11} = 25S_{21}. \tag{2-57}$$

Using third method represented in Fig. 2.9.c, connecting measured two-port network in series with two vector network analyzer ports, S_{21} is measured. Impedance Z_{11} can be calculated, [39]:

$$Z_{11} = 100\frac{1-S_{21}}{S_{21}} = 100\left[\frac{\cos\varphi}{|S_{21}|} - 1 - j\frac{\sin\varphi}{|S_{21}|}\right]. \quad (2\text{-}58)$$

Real part of impedance Z_{11} can be calculated:

$$\mathrm{Re}\{Z_{11}\} = 100\left(\frac{\cos\varphi}{|S_{21}|} - 1\right). \quad (2\text{-}59)$$

Therefore, imaginary part of Z_{11} can be calculated:

$$Im\{Z_{11}\} = 100\frac{-\sin\varphi}{|S_{21}|}. \quad (2\text{-}60)$$

Modulus of impedance Z_{11} can be calculated:

$$|Z_{11}| = 10\sqrt{1 - \frac{2\cos\varphi}{|S_{21}|} + \frac{1}{|S_{21}|^2}}. \quad (2\text{-}61)$$

Absolute error of two-port network $|Z_{11}|$ and $\mathrm{Re}(Z_{11})$ can be calculated using partial derivation. Vector network analyzer, absolute measurement error usually is defined for reflection coefficient and transfer coefficient modulus and phase.

2.6.1 Absolute error of impedance $|Z_{11}|$, $\mathrm{Im}(Z_{11})$ and $\mathrm{Re}(Z_{11})$ using first measurement method

Partially deriving (2-50), (2-50) and (2-52), absolute measurement errors of $|Z_{11}|$, $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ for two- port network, if first measurement method is used, can be calculated:

$$\Delta\mathrm{Re}\{Z_{11}\} = \left|50\frac{-2A|S_{11}| - \left(1-|S_{11}|^2\right)\left(-2\cos\varphi + 2|S_{11}|\right)}{A^2}\Delta|S_{11}| - 50\frac{2\left(1-|S_{11}|^2\right)|S_{11}|\sin\varphi}{A^2}\Delta\varphi\right|,$$

(2-62)

where $A = 1 - 2|S_{11}|\cos\varphi + |S_{11}|^2$,

$\Delta\varphi$- absolute phase error in radians,

$\Delta|S_{21}|$- absolute transfer coefficient error.

$$\Delta \mathrm{I}m\{Z_{11}\} = \left| 100\frac{|S_{11}|\left(A\cos\varphi - 2|S_{11}|(\sin\varphi)^2\right)}{A^2}\Delta\varphi + 100\frac{A\sin\varphi - |S_{11}|\sin\varphi\left(2|S_{11}| - 2\cos\varphi\right)}{A^2}\Delta|S_{11}| \right|.$$

(2-63)

$$\Delta|Z_{11}| = \frac{\mathrm{Re}\{Z_{11}\}\Delta\,\mathrm{Re}\{Z_{11}\} + \mathrm{Im}\{Z_{11}\}\Delta\,\mathrm{Im}\{Z_{11}\}}{|Z_{11}|}. \quad (2\text{-}64)$$

2.6.2 Absolute impedance $|Z_{11}|$, $\mathrm{Im}(Z_{11})$ and $\mathrm{Re}(Z_{11})$ error using second measurement method

Partially deriving (2-54), (2-55) and (2-56) absolute measurement errors of $|Z_{11}|$, $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ for two- port network if second measurement method is used, can be calculated:

$$\Delta\mathrm{Re}\{Z_{11}\} = \left| 25\frac{B\left(\cos\varphi - 2|S_{21}|\right) - \left(|S_{21}|\cos\varphi - |S_{21}|^2\right)\left(2|S_{21}| - 2\cos\varphi\right)}{B^2}\Delta S_{21} - \right.$$
$$\left. - \frac{|S_{21}|B\sin\varphi + 2|S_{21}|\sin\varphi\left(|S_{21}|\cos\varphi - |S_{21}|^2\right)}{B^2}\Delta\varphi \right| \quad (2\text{-}65)$$

$$\Delta|Z_{11}| = 25\left| \frac{\sqrt{B} - |S_{21}|\frac{1}{2\sqrt{B}}\left(2|S_{21}| - 2\cos\varphi\right)}{B}\Delta|S_{21}| - 25\frac{2|S_{21}|^2\sin\varphi}{2B\sqrt{B}}\Delta\varphi \right|, \quad (2\text{-}66)$$

where $B = 1 - 2|S_{21}|\cos\varphi + |S_{21}|^2$.

In case if $|S_{21}| << 1$, then (2-57) can be used. Equation (2-57) can be rewritten in following manner:

$$Z_{11} = 25\,|\,\mathrm{S}_{21}\,|\cos(\varphi) + j25\,|\,S_{21}\,|\sin(\varphi). \quad (2\text{-}67)$$

Therefore, using (2-67) and partial derivation, absolute measurement error of $|Z_{11}|$, $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ can be calculated:

$$\Delta \mathrm{Re}\{Z_{11}\} = 25|\mathrm{S}_{21}|\sin(\varphi)\Delta\varphi + 25\cos(\varphi)\Delta|S_{21}|, \tag{2-68}$$

$$\Delta \mathrm{Im}\{Z_{11}\} = 25|\mathrm{S}_{21}|\cos(\varphi)\Delta\varphi + 25\sin(\varphi)\Delta|S_{21}|, \tag{2-69}$$

$$\Delta|Z_{11}| = 25\Delta|\mathrm{S}_{21}|. \tag{2-70}$$

2.6.3 Absolute impedance $|Z_{11}|$, $\mathrm{Im}(Z_{11})$ and $\mathrm{Re}(Z_{11})$ error using third measurement method

Partially deriving (2-59), (2-60) and (2-61) absolute measurement errors of $|Z_{11}|$, $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ for two- port network, if third measurement method is used, can be calculated:

$$\Delta \mathrm{Re}\{Z_{11}\} = \left| 100\left[\frac{\cos\varphi}{|S_{21}|^2}\Delta S_{21} + \frac{\sin\varphi}{|S_{21}|}\Delta\varphi \right] \right|, \tag{2-71}$$

$$\Delta \mathrm{I}m\{Z_{11}\} = \left| 100\left[\frac{\sin\varphi}{|S_{21}|^2}\Delta S_{21} - \frac{\cos\varphi}{|S_{21}|}\Delta\varphi \right] \right|, \tag{2-72}$$

$$\Delta|Z_{11}| = \frac{5}{|Z_{11}|}\left(\left[\frac{2\cos\varphi}{|S_{21}|^2} - \frac{2}{|S_{21}|^3} \right]\Delta|S_{21}| + \frac{2\sin\varphi}{|S_{21}|}\Delta\varphi \right). \tag{2-73}$$

2.6.4 Measurement method analysis for EMI filter capacitor impedance measurements

Capacitors in EMI filters are low impedance components. Therefore, method used for capacitor impedance measurements should be chosen to provide low error. In Fig. 2.10. capacitor, treated as two-pole network, impedance Z_{11} is measured with all three methods previously described.

Measurement setups are presented in Fig. 2.11. Capacitor capacitance is C=500nF. Three methods give three different results in frequency range, where capacitor has its resonance frequency. At resonance frequency usually ESR of capacitor is graphically determined. It is obvious that the highest error values are in the range of capacitor resonance, where the impedance is very low. In frequency ranges out of capacitor resonance region results are very close for all three measurement methods.

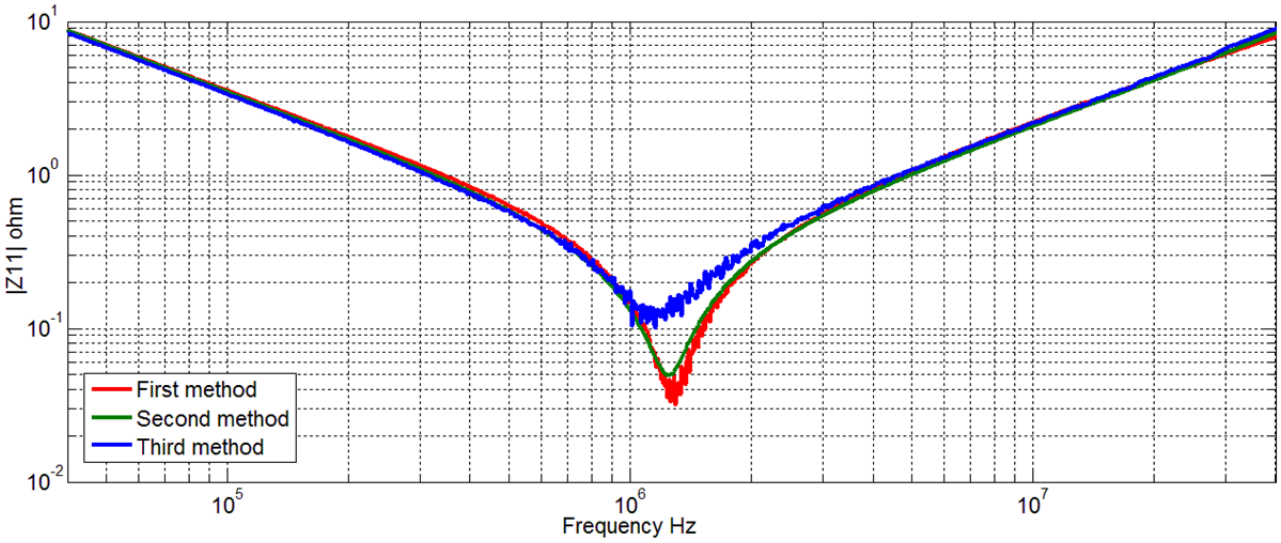


Fig. 2.10. Capacitor measurement using three measurement methods

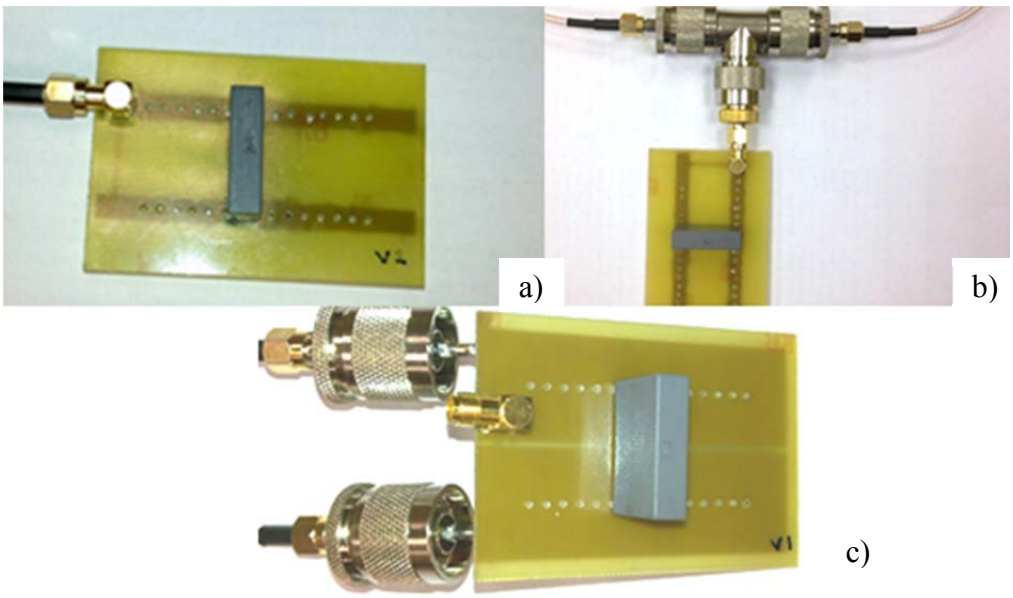


Fig. 2.11. Impedance Z_{11} measurement setups: a) first measurement method, b) second measurement method, c) third measurement method

Vector network analyzer transfer coefficient absolute error is $\Delta|S_{21}|$=0,2dB and absolute phase error is $\Delta\varphi=2^{o}$ in frequency range 20kHz-300kHz. Vector network analyzer transfer coefficient absolute error is $\Delta|S_{21}|$=0.05dB and absolute phase error is $\Delta\varphi=0.4^{o}$ in frequency range 300kHz-50MHz. Vector network analyzer reflection coefficient absolute error $\Delta|S_{11}|$=0.4dB and absolute phase error is $\Delta\varphi=0.3^{o}$ in frequency range 20kHz-50MHz.

Using equations defined in (2-62) to (2-66) and (2-71) to (2-73), measured impedance modulus error and measured real impedance error (ESR relative error) is calculated and plotted for all three measurement methods in Fig. 2.12. to Fig. 2.17.

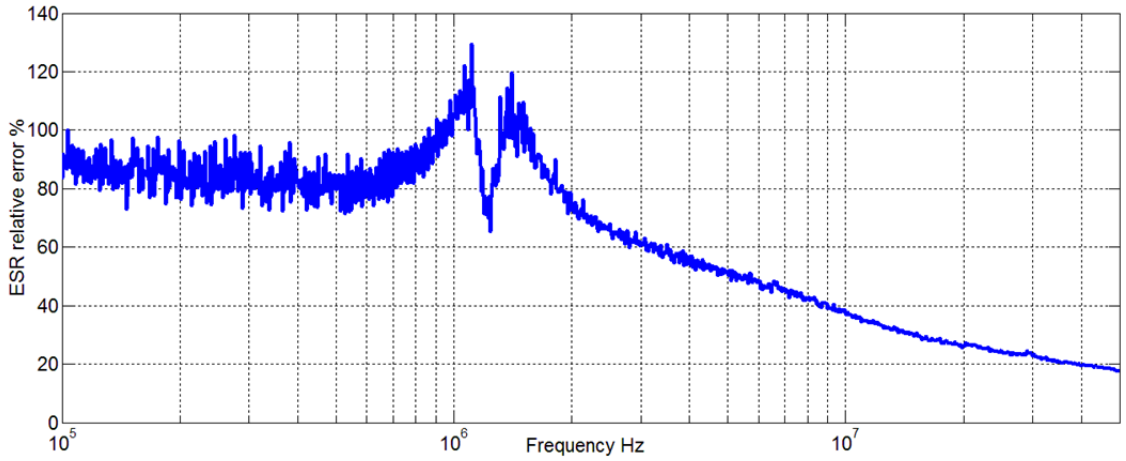


Fig. 2.12. ESR relative error, if first method is used for capacitor measurement

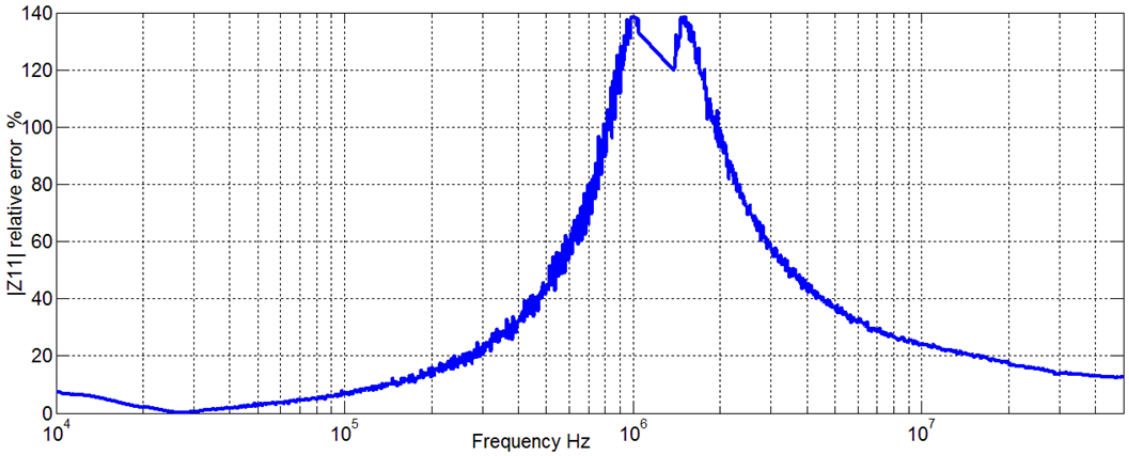


Fig. 2.13. Impedance modulus relative error, if first method is used for capacitor measurement

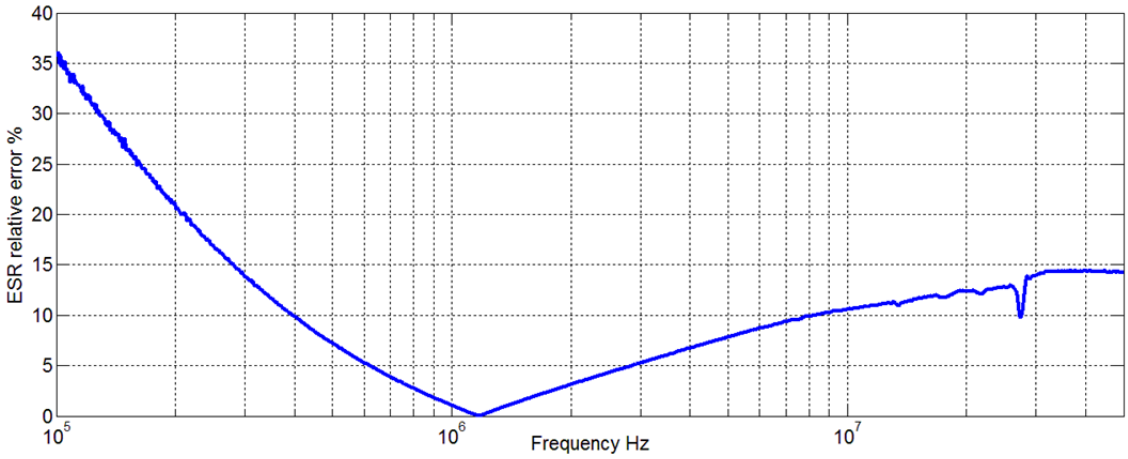


Fig. 2.14. ESR relative error, if second method is used for capacitor measurement

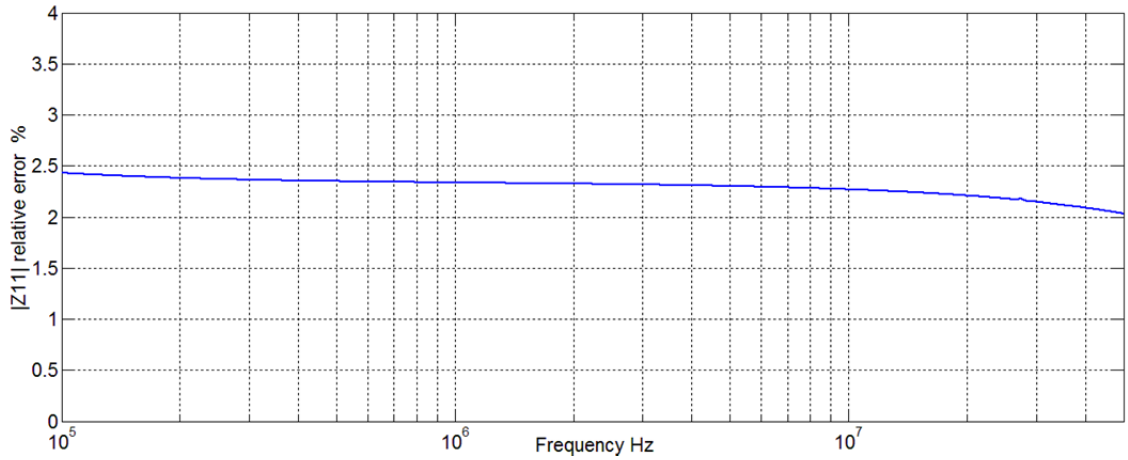


Fig. 2.15. Impedance modulus relative error, if second method is used for capacitor measurement

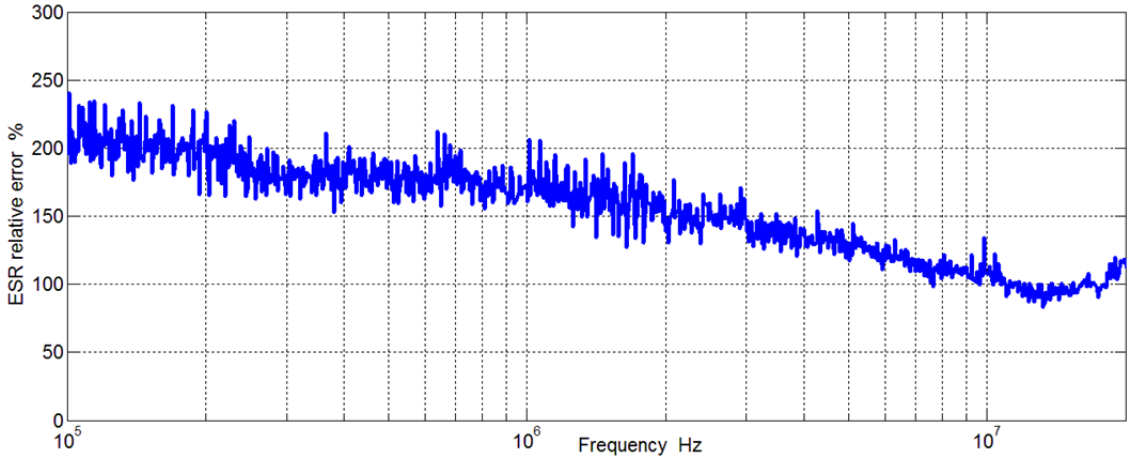


Fig. 2.16. ESR relative error, if third method is used for capacitor measurement

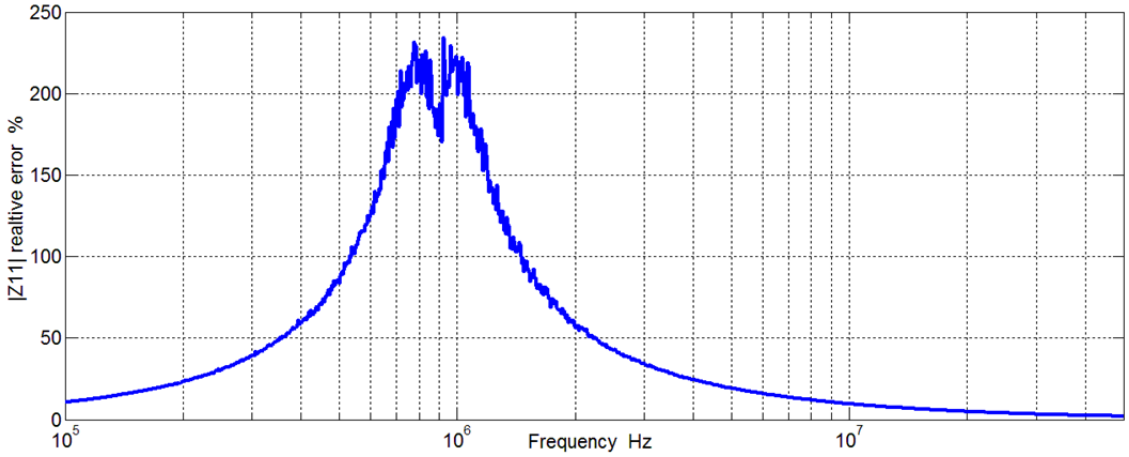


Fig. 2.17. Impedance modulus relative error, if third method is used for capacitor measurement

In case if first method is used in capacitor real impedance Re(Z_{11}) measurement, relative measurement error is higher than 70% up to 2MHz, afterwards it decreases to 20% at 50MHz. It can be explained- due to frequency range (f_{rez}=1.4MHz), that is lower than capacitor resonance frequency, the reflection coefficient $|S_{11}|$ is almost constant and its value is close to 1 and phase is positive, as it can be seen in Fig. 2.18. and Fig. 2.19. But at frequencies higher than capacitor resonance frequency, reflection coefficient $|S_{11}|$ decreases and phase is negative that leads to decrease of measurement error. It is obvious, that this method for EMI filter capacitor Z_{11} measurements is usable only for high frequency measurements, where capacitor impedance is high.

Capacitor series equivalent resistance measurement relative error is high in frequency ranges close to capacitor resonance frequency >50%, but at resonance frequency- ESR, relative measurement error is >100%. At frequencies relatively far from capacitor resonance frequency (<150kHz and >20MHz), ESR relative measurement error is lower than 15%. Relative measurement error dependence of frequency can be explained by the fact, that relative measurement error is proportional to 1/A, were parameter A is defined in (2-62). Parameter A dependence on frequency is calculated and plotted in Fig. 2.20. In frequency range 300kHz-10MHz parameter A value is low and at resonance it is close to 0, therefore relative measurement error is high. In other frequency ranges parameter A value is relatively high and it leads to relative measurement error decrease.

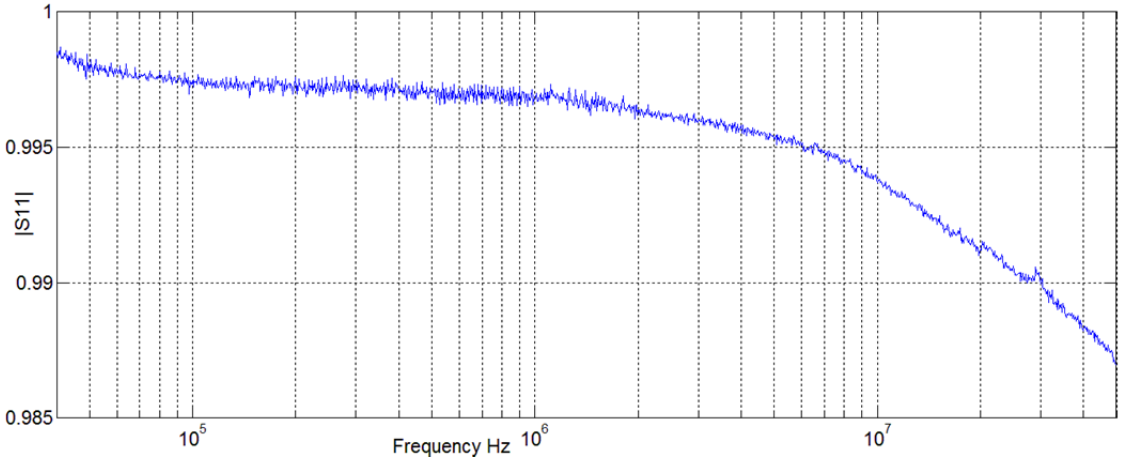


Fig. 2.18. Reflection coefficient $|S_{11}|$ measurement using first measurement method

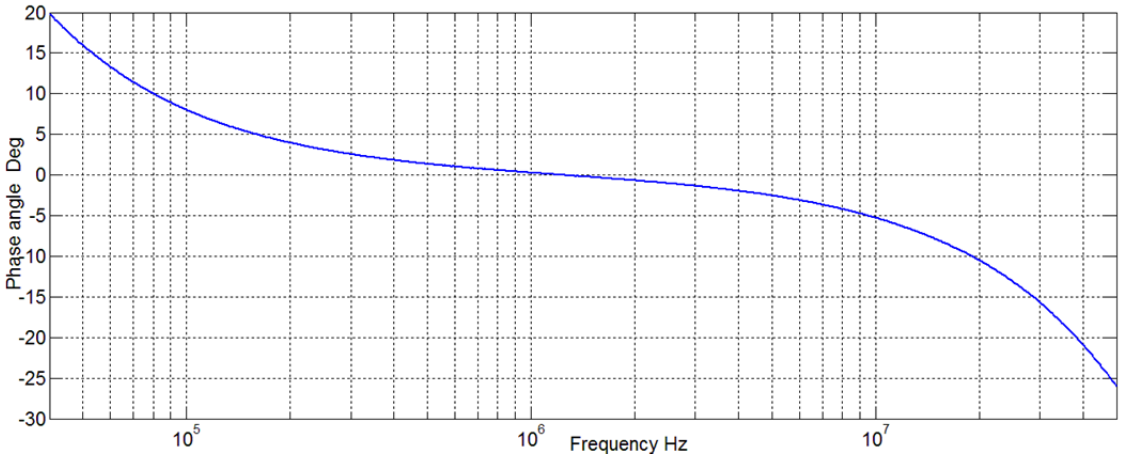


Fig. 2.19. Reflection coefficient $|S_{11}|$ phase measurement using first measurement method

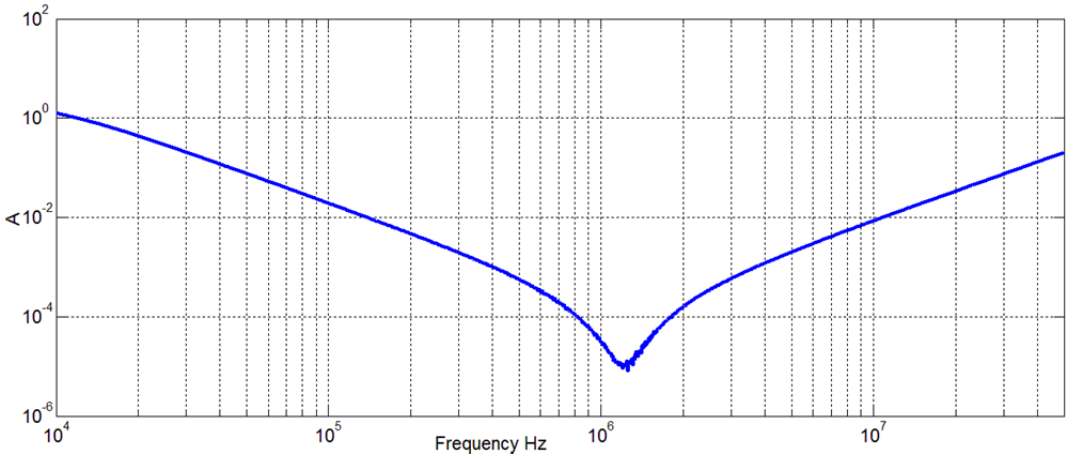


Fig. 2.20. Parameter A calculation using equation (2-62)

Second method has the highest precision for EMI filter capacitor measurements. ESR relative measurement error depends on frequency, as it can be seen in Fig. 2.14. In frequency range that

is close to capacitor resonance frequency (400kHz- 7MHz), relative measurement error is <10%. Closer to resonance frequency relative measurement error is smaller. This can be explained with the fact that ESR relative measurement error is proportional to 1/B, where parameter B is defined in equation (2-66). Parameter B is calculated and plotted in Fig. 2.21. In frequency range 400kHz- 7MHz parameter B value is close to 1 ($|S_{21}|$ is much smaller than 1, Fig. 2.22. and Fig. 2.23.), that leads to low relative measurement error. Capacitor impedance $|Z_{11}|$ relative measurement error does not depend on frequency as it can be seen in Fig. 2.15.

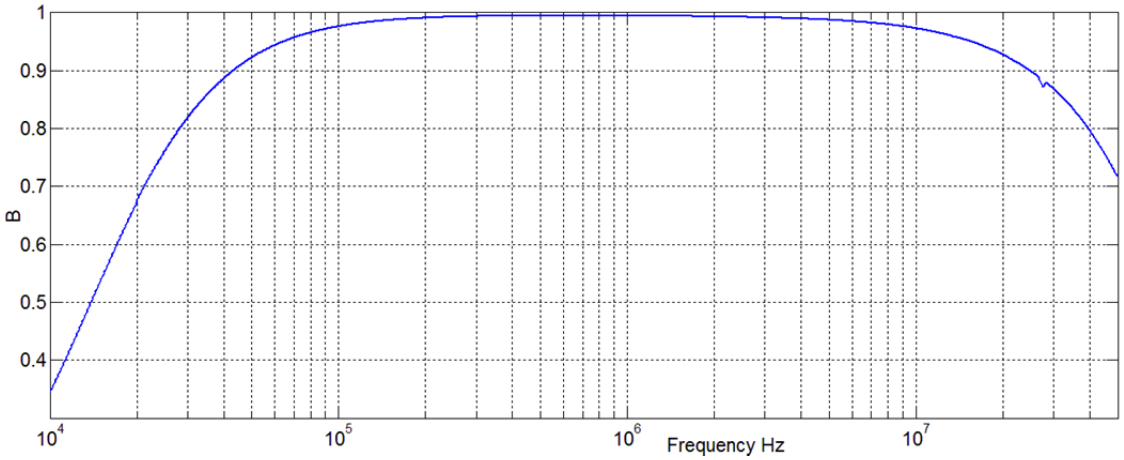


Fig. 2.21. Parameter B calculation using equation (2-66)

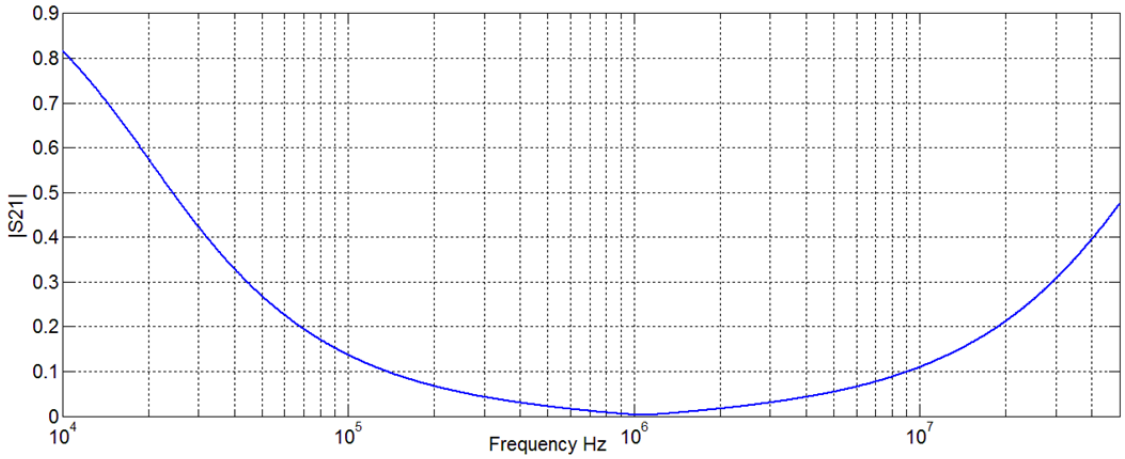


Fig. 2.22. Transfer coefficient $|S_{21}|$ measurement using second measurement method

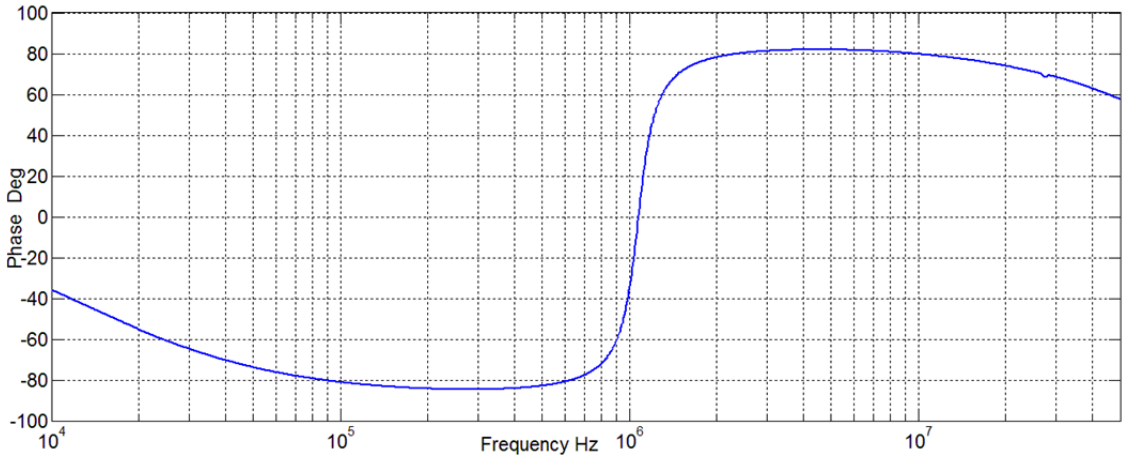


Fig. 2.23. Transfer coefficient $|S_{21}|$ phase measurement using second measurement method

Third method usage in EMI filter capacitor ESR measurements appears to be the worse. ESR relative measurement error is higher than 90% in all frequency range. This can be explained by the fact that $|S_{21}|$ value is close to 1 (0dB), Fig. 2.24. and Fig. 2.25.

Capacitor impedance $|Z_{11}|$ relative measurement error similarly as in first method depends on frequency. Impedance $|Z_{11}|$ relative measurement error rises with the frequency- reaching the maximal value 240%, at the capacitor resonance frequency, afterwards relative measurement error decreases Fig. 2.17.

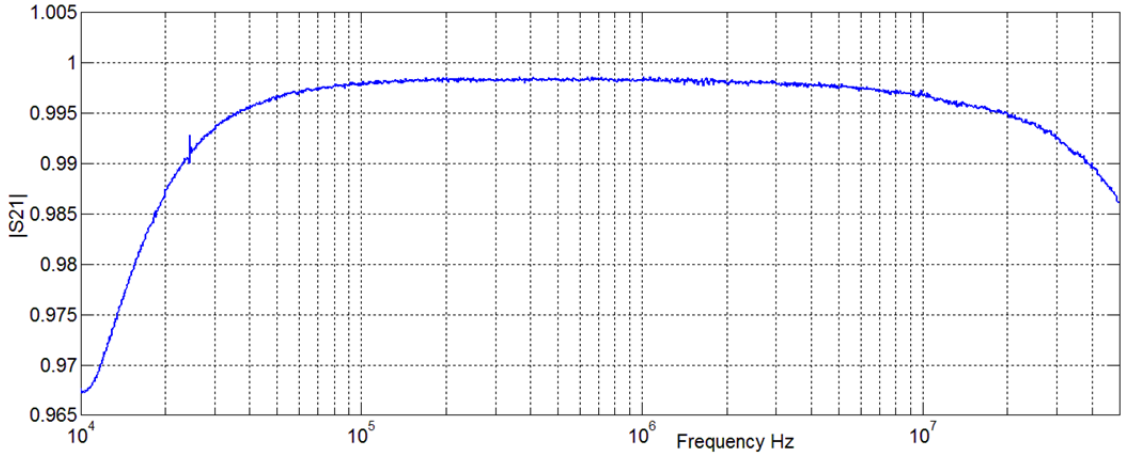


Fig. 2.24. Transfer coefficient $|S_{21}|$ measurement using third measurement method

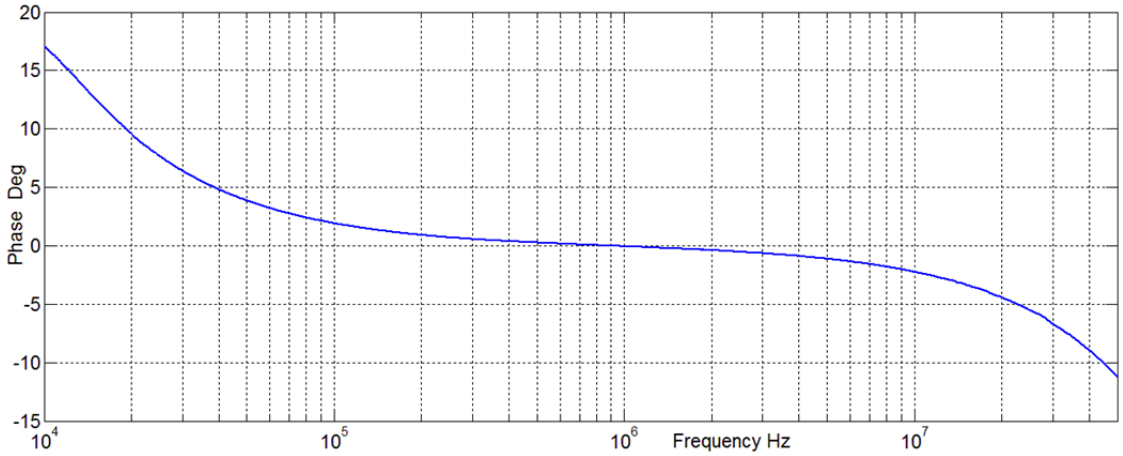


Fig. 2.25. Transfer coefficient $|S_{21}|$ phase measurement using third measurement method

2.7 Filter inductor impedance measurements using scattering parameters

Inductors, Fig. 2.26., are used in electronics for many purposes. One of the fields is electromagnetic compatibility filters. The main parameters for inductor used in EMI filters are:

L- inductance,

$|Z_L|$- impedance modulus,

f_{rez} - self-resonance frequency.

Fig. 2.26. Inductor

Real inductor depending on construction has a couple of parasitic parameters:

ESR- equivalent series resistance, that describes losses in copper and core material,

EPC- equivalent series capacitance, that describes winding self-capacitance,

EPR- equivalent parallel resistance.

Self-resonance of inductor can be calculated using:

$$f_{rez} = \frac{1}{2\pi\sqrt{L \times EPC}}. \tag{2-74}$$

Real inductor simple lumped element model is given in Fig. 2.8.b. In Fig. 2.27. inductor impedance is plotted in frequency range. At inductor resonance frequency- f_{rez}, inductor impedance reaches the highest value. If $f<f_{rez}$, then $|Z_L|$ rises and if $f>f_{rez}$, then $|Z_L|$ decreases. Inductor impedance can be described in the following complex form:

$$Z_L = \frac{R + j2\pi fL}{1 - (2\pi f)^2 L \times EPC + j2\pi f \times ESR \times EPC}. \tag{2-75}$$

Inductor model represented in Fig. 2.8.b do not take into account inductor series resonance, created by component leads inductance.

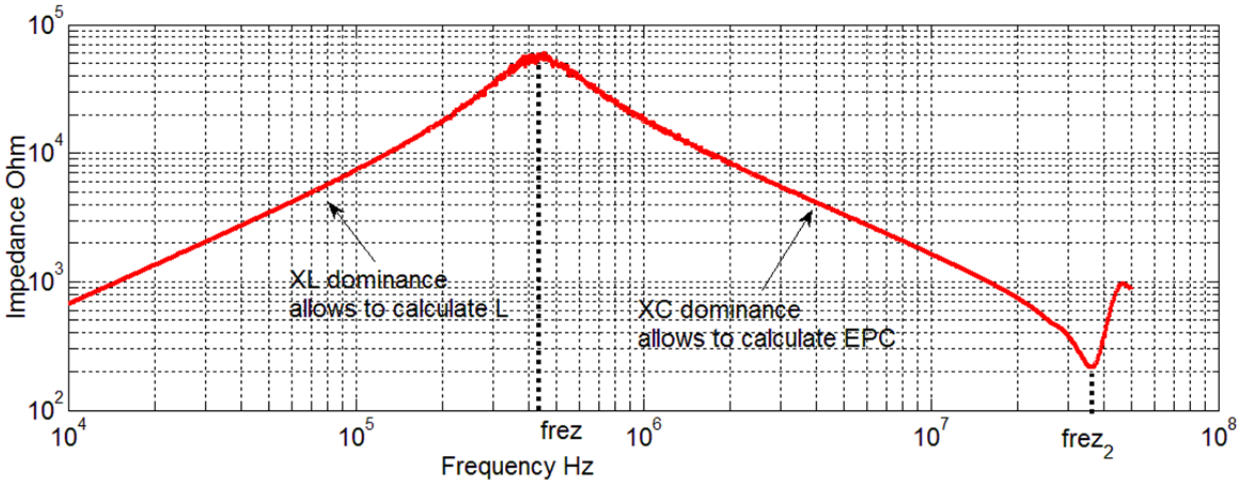


Fig. 2.27. Inductor impedance plot

At series resonance frequency- f_{rez2}, inductor impedance $|Z_L|$ reaches the lowest value. Therefore, it is necessary to improve current inductor lumped element model by adding series inductance L2, representing component leads inductance, as in Fig. 2.28. Inductor lumped element model becomes complex doe to the increase of component physical complexity- multiple turns, complex core geometry, long leads. If magnetic core is used, lumped element model parameter- L is frequency dependent, as it depends on magnetic material properties. L2 and EPC are not frequency dependent and these values are defined by component geometry.

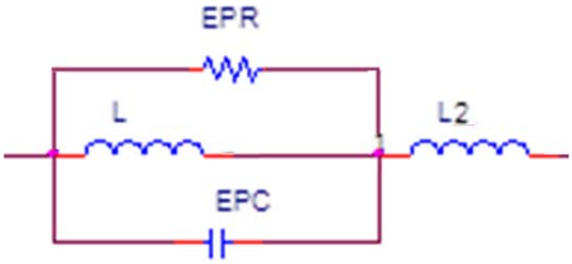


Fig. 2.28. Improved inductor lumped element model

Inductor impedance described by lumped element model shown in Fig. 2.28, can be calculated in the following complex form:

$$Z_{\mathrm{L}} = \frac{1}{\frac{1}{ESR} + \frac{1}{j2\pi fL} + j2\pi f \times EPC} + j2\pi fL_1. \tag{2-76}$$

Capacitance EPC can be calculated from the linear $|Z_L|$ region, where impedance X_C is dominating, (Fig. 2.27.):

$$EPC = \frac{1}{2\pi f_1 \mid Z_L(f_1) \mid}, \tag{2-77}$$

where

f_1 - frequency in linear region of $| Z_L |$,

$| Z_L(f_1) |$ - impedance at frequency f_1.

If series self-resonance of inductor is known, parasitic inductance L_1 can be calculated using Thomson equation for resonance:

$$L_1 = \frac{1}{4\pi^2 f_{rez2}^2 EPC}. \tag{2-78}$$

Inductance L is frequency dependent, as inductor is created with ferrite core. Inductance L can be calculated from the linear $|Z_L|$ region, where X_L is dominating:

$$L = \left| \frac{1}{2\pi f \left[\mathrm{Im}\left\{ \frac{1}{Z_L - j2\pi f L_1} \right\} - 2\pi f EPC \right]} \right|. \tag{2-79}$$

Therefore, EPR can be calculated:

$$EPR = \frac{1}{\mathrm{Re}\left\{ \frac{1}{Z_L - j2\pi f L_1} \right\}}. \tag{2-80}$$

2.7.1 Measurement method analysis for EMI filter inductance impedance measurements

If inductor is treated as two port network it is enough to measure impedance Z_{11} that gives enough data to calculate its parameters. There are three impedance Z_{11} measurement methods for two port networks represented in Fig. 2.9., that utilize vector network analyzer. Therefore, it is important to analyze them and to choose the proper one to obtain results with highest precision.

There are three methods for inductor Z_{11} measurement:

1. Reflection coefficient- S_{11}, measurement using one vector network analyzer port, if two port network is connected in parallel to the vector network analyzer port, Fig. 2.9.a,
2. Reverse transmission coefficient- S_{21}, measurement if two port network is connected in parallel with the vector network analyzer ports, Fig. 2.9.b;
3. Reverse transmission coefficient- S_{21}, measurement if two port network is connected in series with the vector network analyzer ports, Fig. 2.9.c;

Measurement error of Z_{11} can be very high if $|S_{11}|$ and $|S_{21}|$ is close to 1 (0dB). Therefore, measurement method selection depends on measured impedance magnitude. Inductor impedance usually is high, therefore, second method usage is not recommended. Second method can be used

if low impedance inductors should be analyzed. For inductor measurements first and third method is more suitable. Inductor measurement setups are presented in Fig. 2.29. and measurement results are compared in Fig. 2.30. At frequencies that are apart from inductor impedance resonance frequency, the difference between measurements is in range of 10%. The highest difference between two measurements is in range of inductor impedance resonance frequency, where it reaches 30%. The first method in frequency range close to inductor impedance resonance frequency gives noisy measurement results. Inductor parameters are compared in Table 2.1. for both methods. Inductance L_{eff} were measured also with LRC analyzer Instek LRC-819. L_{eff} measurement results using LRC analyzer and calculation results using first and third method at 100kHz, agree very well. Difference between first and third measurement method predicted inductor impedance resonance frequency is up to 15%. This can be explained by the fact that measurement error using first measurement method next to resonance frequency is high (measurement error is high if measured impedance is high).

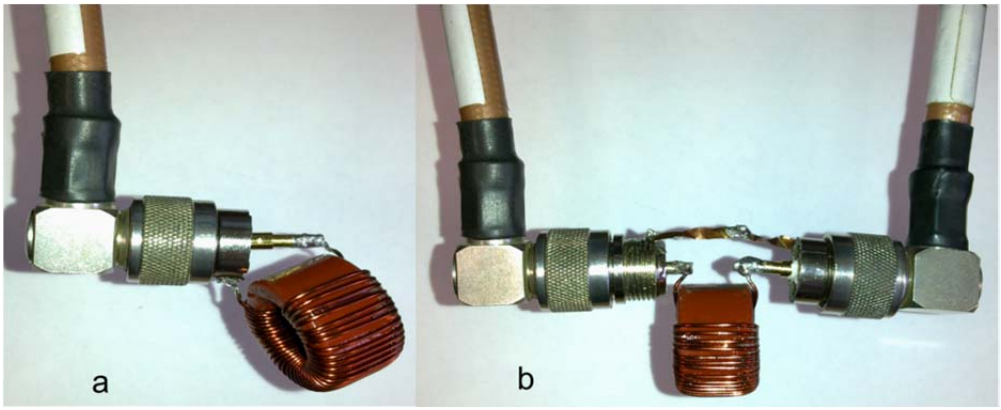


Fig. 2.29. Test setup: a) first measurement method; b) third measurement method

Using equations (2-79) and (2-80), inductor inductance and equivalent parallel impedance are calculated using results obtained by third measurement method. Results are presented in Fig. 2.31. and Fig. 2.32.

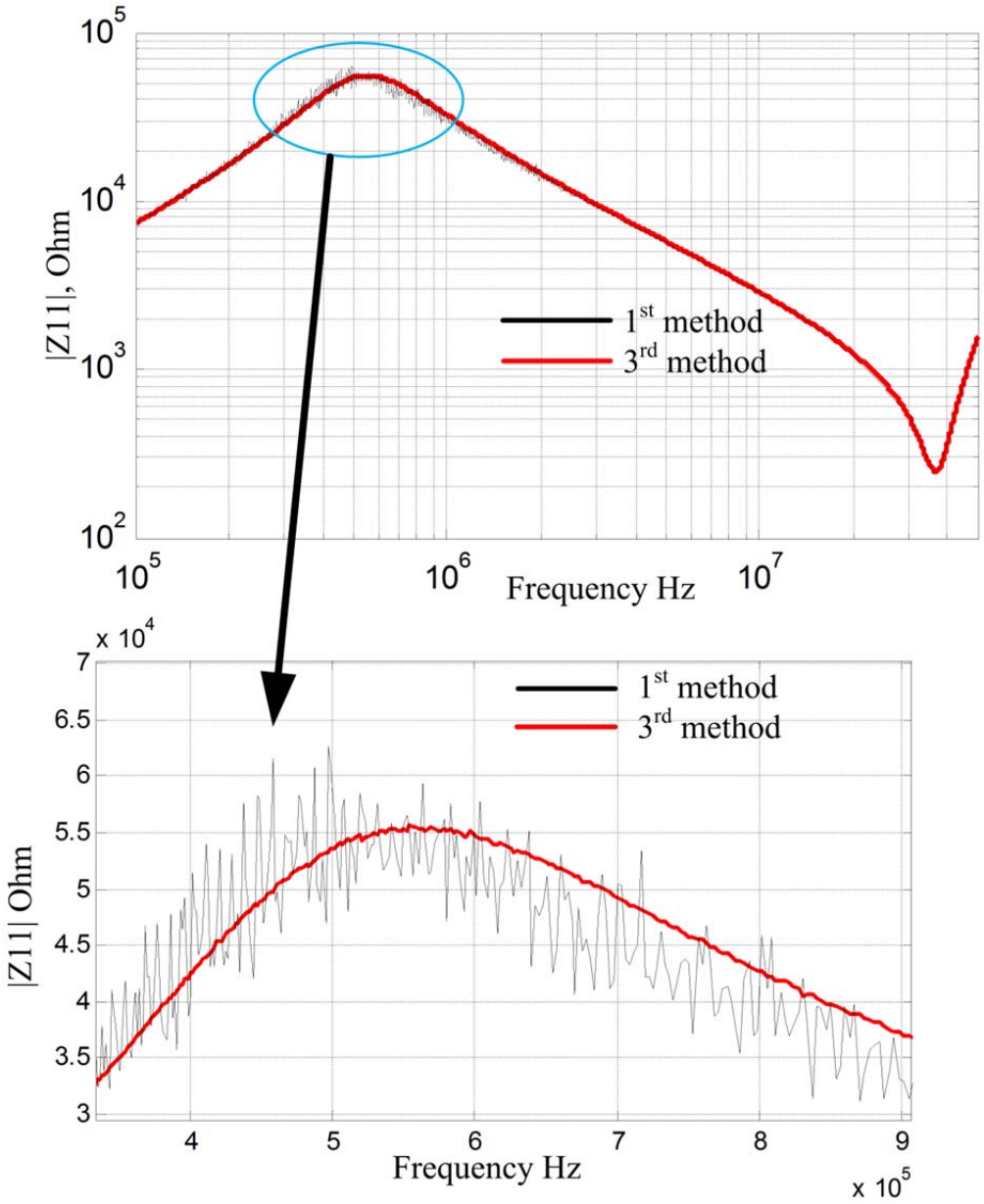


Fig. 2.30. Inductor impedance measurements with first and third measurement method

Table 2.1.

Inductor measurement results obtained by VNA and LRC analyzer

	VNA measurements		LRC analyzer measurements
	1st method	3rd method	
$L_{f=100kHz}$, mH	11,48	11,59	11,60
f_{rez}, kHz	497,4	554,5	-

f_{rez2}, MHz	36,5	37	-
EPC, pF	5,7	5,4	-
L_1, µH	3,3	3,4	-

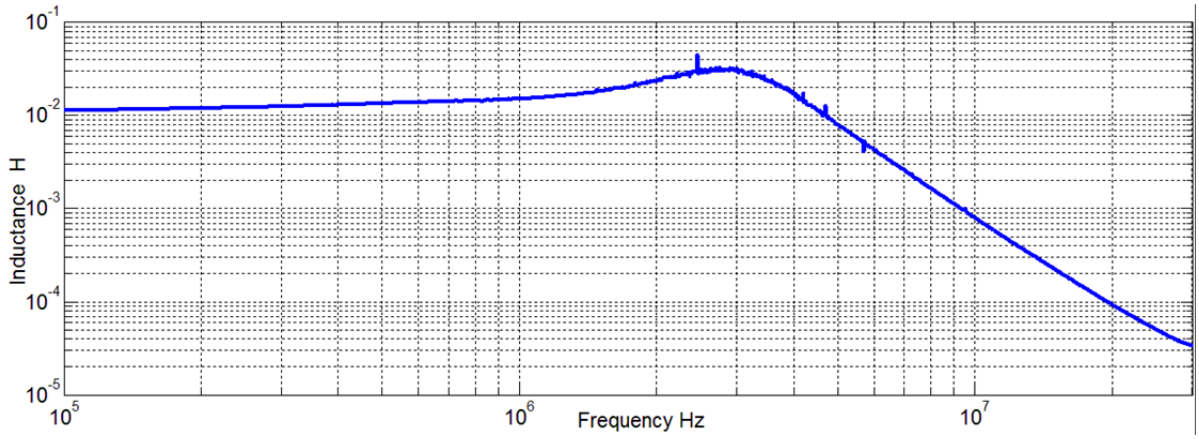


Fig. 2.31. Calculated inductor inductance using results obtained by third measurement method

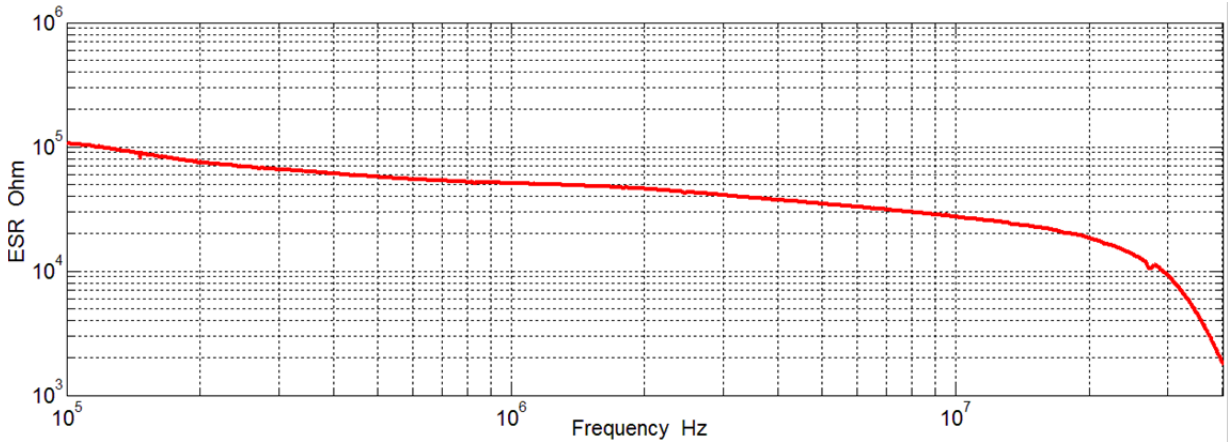


Fig. 2.32. Calculated inductor equivalent parallel resistance using results obtained by third measurement method

Inductor impedance measurement error can be calculated using equation (2-64), for first measurement method. If third measurement method is used equation (2-73) can be used to calculate inductance measurement error.

Inductor, shown in Fig. 2.26., inductance has been calculated at 100kHz (L=11,6mH). Using vector network analyzer datasheet [40], $|S_{21}|$ error can be determined. In frequency range 20kHz-300kHz it is $\Delta|S_{21}|$=0,2dB and in frequency range 300kHz-50MHz $|S_{21}|$ measurement error is $\Delta|S21|$=0,05dB. Phase absolute error $\Delta\varphi=0{,}4^0$. Reflection coefficient $|S_{11}|$ measurement error in whole frequency range is $\Delta|S_{11}|$=0,4dB and absolute phase measurement error is $\Delta\varphi=3^0$.

Using equation (2-64) and equation (2-73) impedance relative measurement error are calculated and shown in Fig. 2.33. and Fig. 2.34.

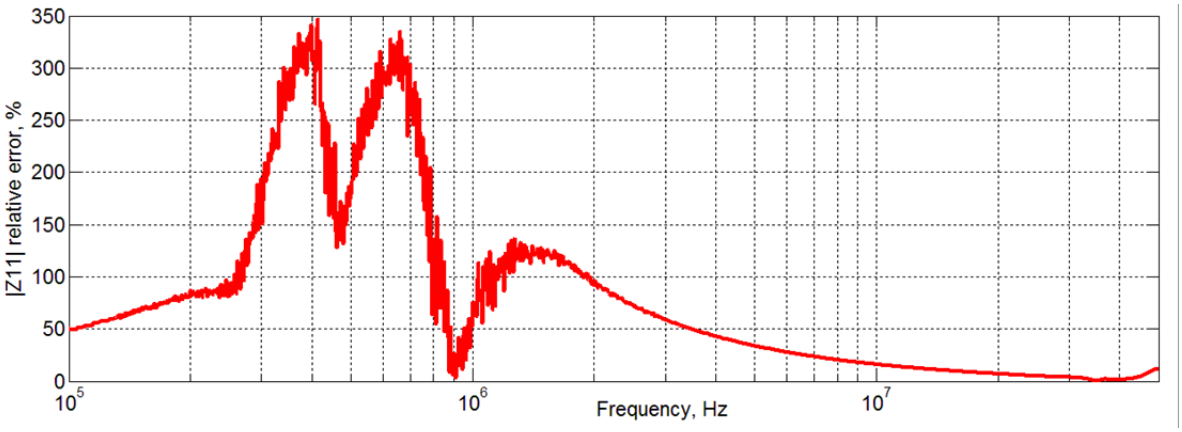


Fig. 2.33. Inductor impedance relative measurement error for first measurement method

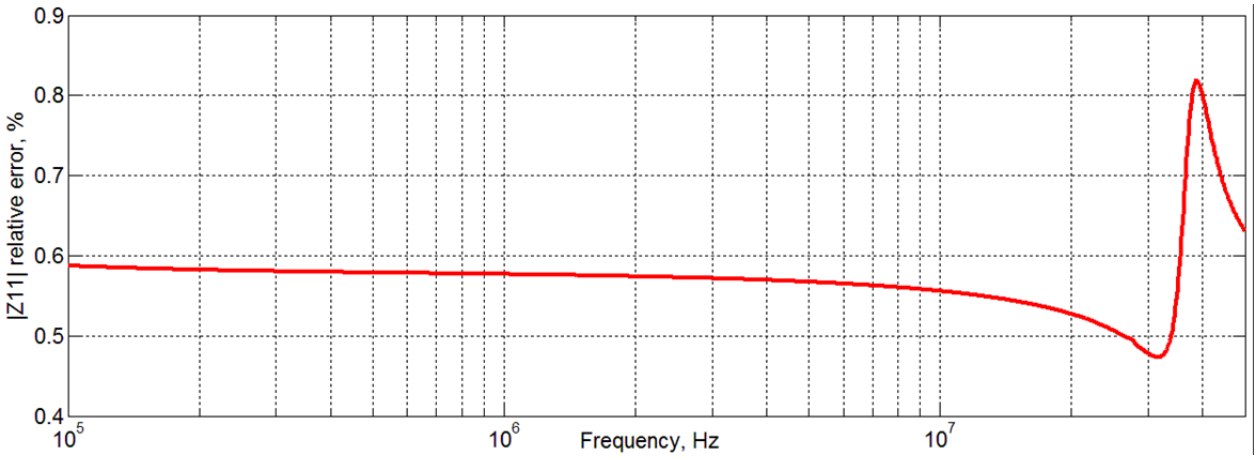


Fig. 2.34. Inductor impedance relative measurement error for third measurement method

Inductor impedance relative measurement error for first measurement method is high, especially next to impedance resonance. Third measurement method gives results with relative measurement error lower than 1% in whole frequency range. Despite the high relative measurement error of first measurement method, if results are compared, difference between impedance delivered by both measurement methods is negligible, as can be seen in Fig. 2.30. Negligible difference can be explained by fact that vector network analyzer measurement error is lower than defined in the datasheet. In datasheet the maximal error is defined, but usually measurement error is much lower.

2.8 Conclusions

In measurement equipment market, dedicated impedance analyzers for high frequencies are rare and expensive items. For impedance measurement purposes vector network analyzer can be utilized. There is a huge offer in the market of vector network analyzers for lower prices than impedance analyzers. Therefore, scattering parameter usage in EMI filter characterization and filter component characterization methods are developed and measurement errors are analyzed in this chapter.

International standard CISPR 17 defines EMI filter insertion loss measurement methods. The recent version of CISPR 17 already includes measurement methods if vector network analyzer is used. Component analysis methods using vector network analyzer also are included in CISPR 17, but there is no analysis of errors for different measurement methods. In this chapter different measurement methods have been analyzed and suitable methods for EMI filter capacitive and inductive components selected.

The most suitable method for EMI filter capacitor measurement is reverse transmission coefficient- S_{21}, measurement if two capacitors are connected in parallel with the vector network analyzer ports as in Fig. 2.9.b. Relative impedance measurement error for this method is below 2.5%, in comparison to other methods that gives error up to 250%.

The most suitable method for EMI filter inductive component measurements is reverse transmission coefficient- S_{21}, measurement if inductive component is connected in series with the vector network analyzer ports, Fig. 2.9.c. Relative impedance measurement error for this method is below 1%, in comparison to other methods that give error up to 350%.

3. EFFECTS OF PARASITIC COMPONENT PARAMETERS ON THREE PHASE Π TYPE EMI FILTER

3.1 Background

In electromagnetic interference (EMI) passive filter design, it is well known fact, that component parasitic parameters, such as parasitic inductance of capacitors and parasitic winding capacitance of chokes and their self-resonant effect, play important role in filter performance, however these obstacles engineers can easily avoid due to high quality components, whose are supplied width datasheets with included high frequency parasitic parameters. Based on these parasitic parameters a high frequency filter models can be created and filter performance can be verified and tuned up before the filter is included in a real product. Another problem in EMI filter design is related to parasitics connected to component layout, packaging and routing on the PCB board. Although this problem can be solved theoretically using field simulation software, the nowadays filter design is characterized by a trial and error process which is the more efficient the more experienced the designer is. In Fig. 3.1. the situation is explained in terms of filter forward insertion gain. There is plotted modeled ideal three phase filter differential mode (DM) forward insertion gain shown in Fig. 3.2., consisting of ideal components without parasitic elements such as equivalent series resistance, equivalent series inductance, equivalent parallel capacitance, equivalent parallel resistance (ESR, ESL, EPC, EPR). In real life, filters are mounted on PCB's, Fig. 3.3., Fig. 3.4. and have array of parasitics. There is plotted modeled three phase filter DM forward insertion gain shown in Fig. 3.5. (mutual couplings between components are not taken into account). For reference there is plotted measured forward insertion gain of the filter with same circuit that shows the importance of the effects of parasitic parameters (mutual coupling) on EMI filter performance, especially in high frequency range. The difference between the forward insertion gains is negligible up to frequency of 600kHz, where the dominant is component expected values, such as, capacitor capacitance and inductor inductance. In high frequency region various filter component parasitics as well as mutual couplings between components take precedence and greatly affect the amplitude of filter gain.

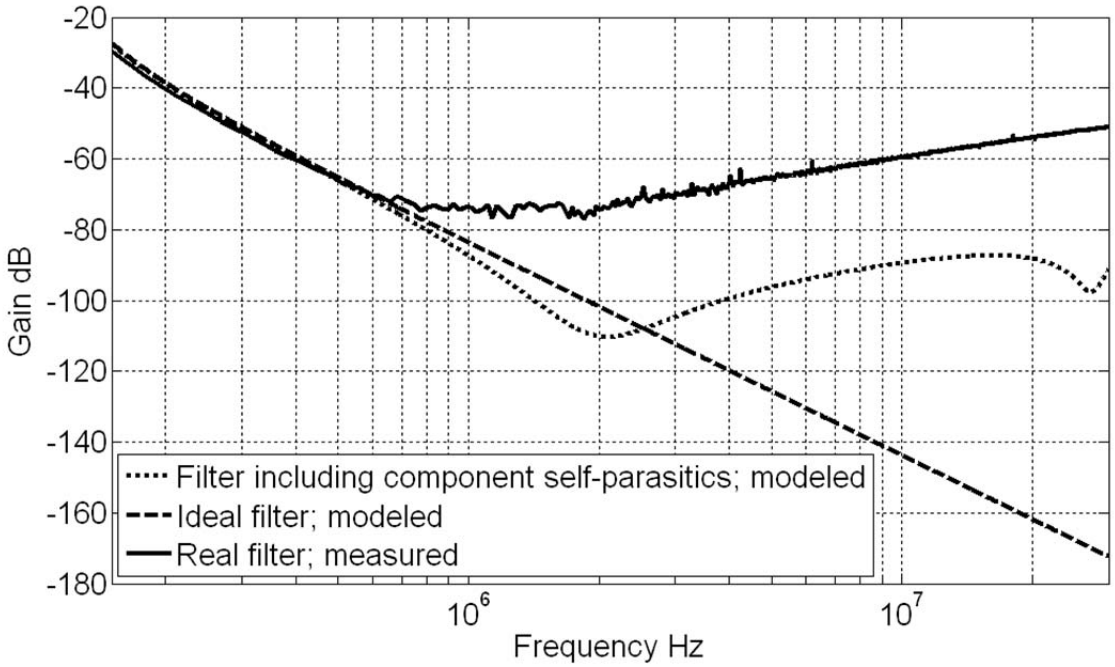


Fig. 3.1. Three phase filter forward insertion gain

This chapter is devoted to the investigation of three phase power electronic filter layout related problems created by parasitics between filter components and self-parasitic components of PCB. It will be shown that these parasitics have a serious influence on three phase filter gain and that a filter with identical components and identical topology can exhibit different performance in disturbance attenuation due to layout of PCB. Research will be done based on real three phase filer prototypes, from a real circuit standpoint so that results and conclusions can be transferred to many practical problems associated with three phase filter component placement and PCB layout considerations. The investigation will be done on six coupling effects, similarly classified as for one phase filters in [41]:

- mutual inductance between common mode choke and capacitor branch,
- mutual inductance between two capacitor branches,
- mutual inductance between common mode choke and PCB ground layer,
- mutual inductance between common mode choke and PCB traces,
- mutual inductance between in and out trace loops,
- coupling capacitance between PCB traces.

3.2 Three phase filter parasitic couplings

Typically used three phase filter for power electronic EMC problem mitigation are shown in Fig. 3.2. Capacitor branch C1 consists of capacitors C11 C12 C13 and capacitor branch C2 consists of capacitors C21 C22 C23. They are used for differential mode (DM) disturbance attenuation, the capacitance is 0.47uF. Common mode (CM) choke is used for CM disturbance mitigation. Practically the CM inductance of a three phase CM choke is the inductance of its three coils connected in parallel [42]. While the mutual magnetic coupling adds to the inductance for CM disturbance, the magnetic flux of DM disturbance cancel each other out. Only the leakage of three phase inductance is magnetized by DM currents. As the power carrying nominal current is a DM signal the leakage inductance is an important parameter and may not be too big to prevent core saturation. On the other hand leakage inductance is a useful parasitic element to attenuate DM disturbance at higher frequencies. Inductance of CM part of choke is L_{cm}=0.2mH and leakage inductance that couples in to the air and other components L_{dm}=6.45uH for the horizontal alignment and L_{cm}=0.22mH, L_{dm}=7.67uH for vertical alignment choke respectively.

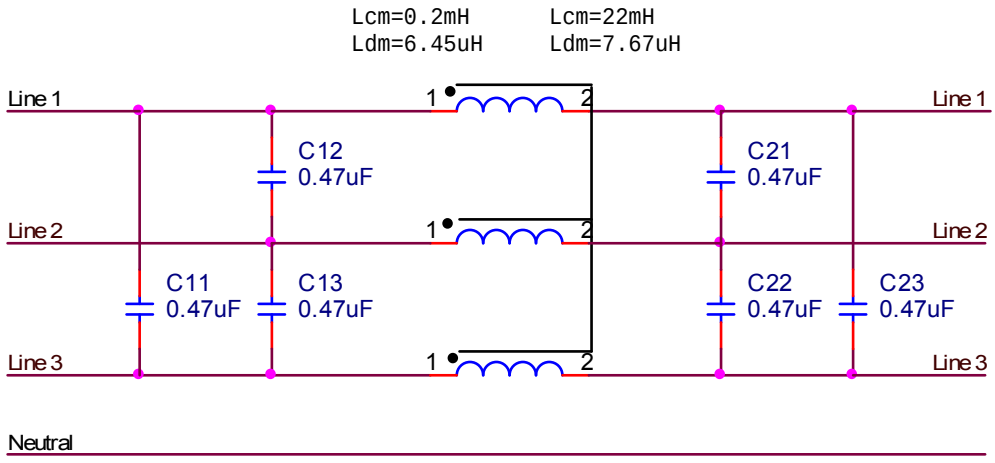


Fig. 3.2. Three phase filter prototype schematic

Two filter prototypes are shown on Fig. 3.4. with vertical CM choke and horizontal CM choke. Both filters have the same capacitors and PCB layout, as shown in Fig. 3.3. PCB contains two layers. The red collared layer is used for component wiring and blue collared layer is used as ground plane. Similar PCB without ground plane has been made due to measurement procedure requirements, explained in details further in this chapter.

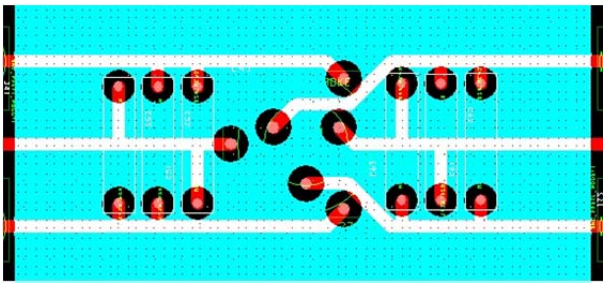


Fig. 3.3. Three phase filter prototype printed circuit board

DM part of three phase filter schematic with extracted component self-parasitics is shown in Fig. 3.5. ESR and ESL are parasitic elements of capacitor, respectively, equivalent series resistance and equivalent series inductance. EPR and EPL are parasitic of CM choke, respectively, equivalent parallel resistance and equivalent parallel inductance.

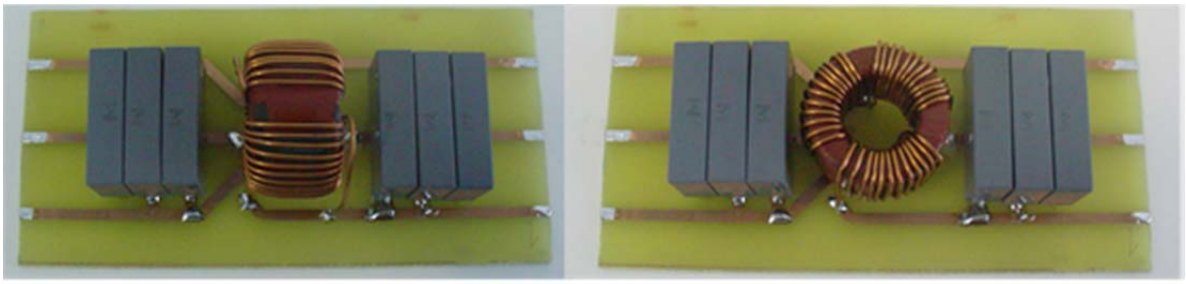


Fig. 3.4. a) Filter prototype with vertical CM choke b) Filter prototype with horizontal CM choke

It is inordinate to show all the couplings between all filter components, because of the large quantity of them. DM filter model is developed for the filter each phase separately. Due to, all phase components are equal it is reasonable to show only one of them with all couplings that are investigated in this chapter. Although components of filter are equivalent the values of couplings are variable phase to phase, due to layout of PCB and component placement. One phase DM filter model as described in [43] and [44] is shown in Fig. 3.6.

There are two types of coupling: capacitive coupling and inductive coupling. Inductive coupling has a significant impact on small current branches if in close proximity there are large current branches, i.e., current branches have great current difference. Capacitive coupling has significant impact on junctions with lower potential if in close proximity there are junctions with high potential, respectively, junctions are with great potential difference. In three phase filter, inductive coupling, such as coupling between CM choke and capacitors, capacitor and capacitor, input and output trace loops, has a large impact on filter gain.

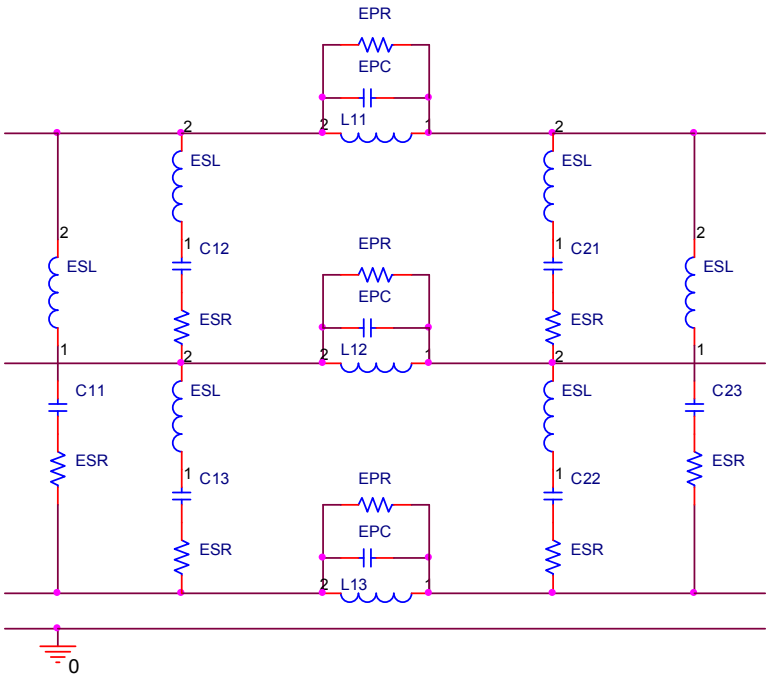


Fig. 3.5. Three phase filter with extracted component parasitic elements

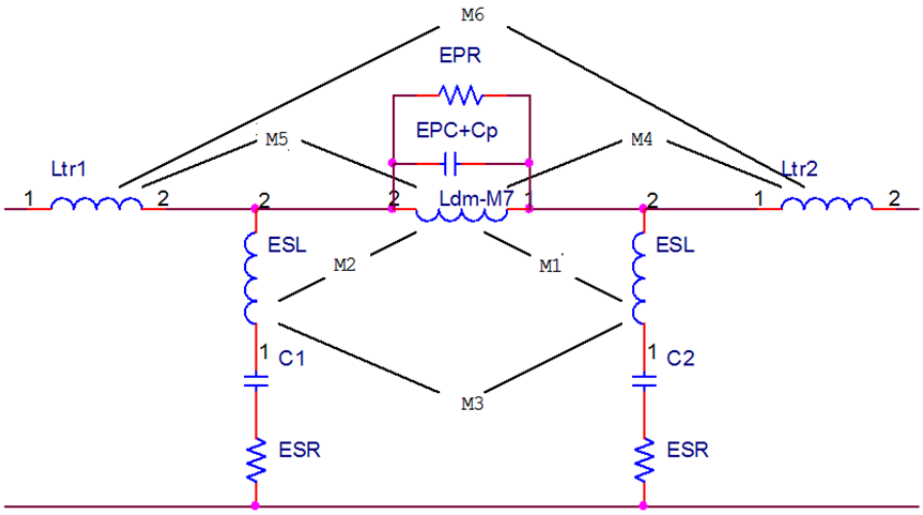


Fig. 3.6. Differential mode model of three phase filter, one phase

Also capacitive coupling between input and output has a large impact on three phase filter performance. Ltr1 and Ltr2 are input and output trace loops created by PCB layout. M1 and M2 are mutual inductance between CM choke and capacitor branches C1 and C2. M3 is the mutual inductance between two capacitor branches C1 and C2. M4 and M5 are mutual inductance between CM choke and input/output trace loops, L_{tr1} and L_{tr2}. M6 is mutual inductance between input/output trace loops, L_{tr1} and L_{tr2}. M7 is mutual inductance between CM choke and ground plane, more precisely, M7 is equivalent inductance reduction of CM choke differential mode

inductance- Ldm, due to eddy current losses in ground plane. Cp is parasitic capacitance between input and output of the filter. Cp is added in parallel with CM choke equivalent parallel capacitance.

3.3 Inductive coupling between CM choke and capacitors and between CM choke and input/output loops

The couplings between CM choke leakage inductance and other inductive parts of three phase filter, such as capacitors, PCB traces and PCB ground plane have common circuitry relationship- coupled inductors. It is not straightforward to set up mesh equations or node equations for circuits containing coupled coils. It is much easier if pair of coupled inductors is replaced by equivalent that contains uncoupled inductors.

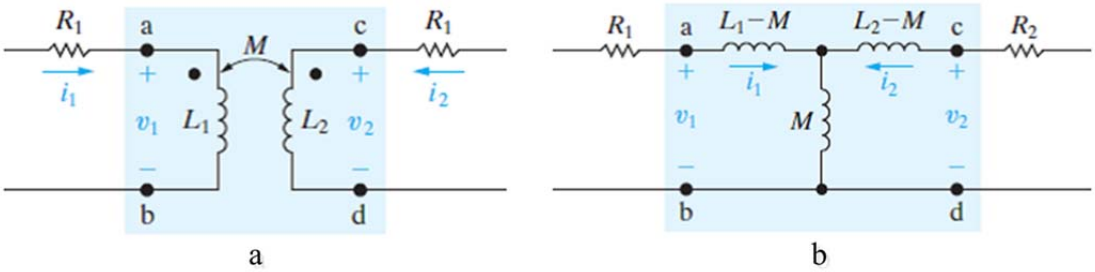


Fig. 3.7. a) Coupled inductors b) Equivalent without coupled inductors

It is possible to write two differential equations that relate the terminal voltages v1 and v2 to terminal currents i1 and i2 in Fig. 3.7.a, for the given references and polarity dots:

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \ , \tag{3-1}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \ , \tag{3-2}$$

where v_1, v_2- inductor terminal voltage,

L_1, L_2- inductor inductance,

i_1, i_2- inductor current.

To make an equivalent circuit for these two magnetically coupled coils, an arrangement of inductors should be defined that can be described by a set of equations equivalent to (3-1) and (3-2). Equations (3-1) and (3-2) can be rewritten as:

$$V_1 = j\omega L_1 I_1 + j\omega M I_2 = j\omega(L_1 - M)I_1 + j\omega M(I_1 + I_2) \ , \tag{3-3}$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2 = j\omega M(I_2 + I_1) + j\omega(L_2 - M)I_2 \ . \quad (3\text{-}4)$$

Therefore, the equivalent T-network for the coupled inductors is shown in Fig. 3.7.b. If coupling of the inductors is different, the dots of any one of the windings are placed in the opposite end of the coil, the coupling becomes negative and equivalent circuit can be obtained by replacing M by $-M$. In this case, the three inductances in Fig. 3.7.b changes to $L_1 + M;\ -M;\ L_2 + M.$

Taking into account the equivalent coupling polarities, the capacitor branch and CM choke, input/output trace loops and CM choke, equivalent circuits are developed in Fig. 3.8., Fig. 3.9. and Fig. 3.10. [41]. Considering different coupling polarities, two circuits for each case are developed and their equivalent circuits for couplings, on the right, respectively. Coupling is called positive, if the capacitor branch equivalent inductance is positive and coupling is called negative if the capacitor branch equivalent inductance is negative. In the case if both couplings exist at the same time, the total effect determinates the coupling polarity. One of the coupling possibilities is shown on Fig. 3.10. (coupling between input/output trace loop and capacitor branch is insignificant and it is out of the scope of this research).

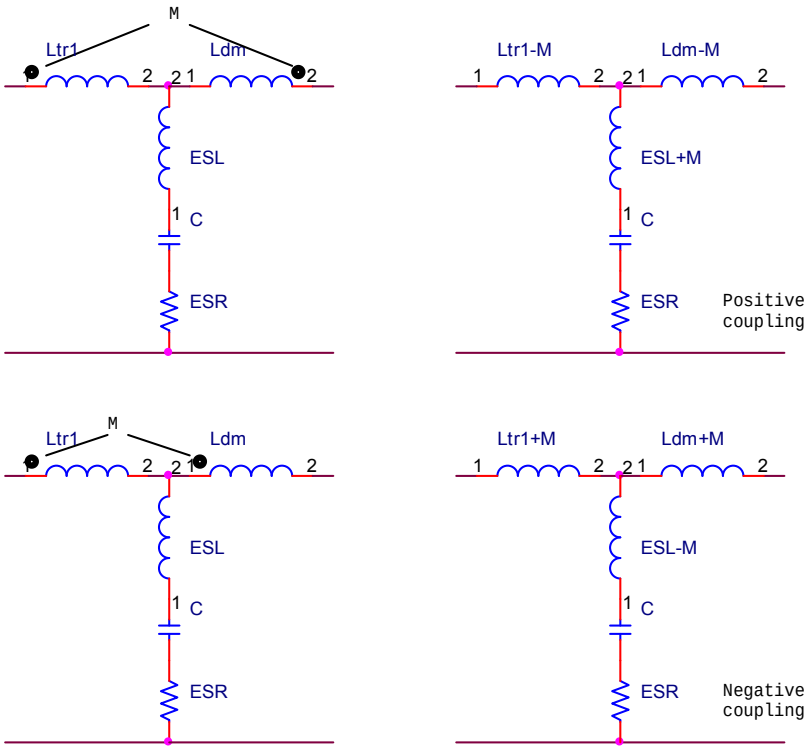


Fig. 3.8. Coupling between input/output trace loop and CM choke

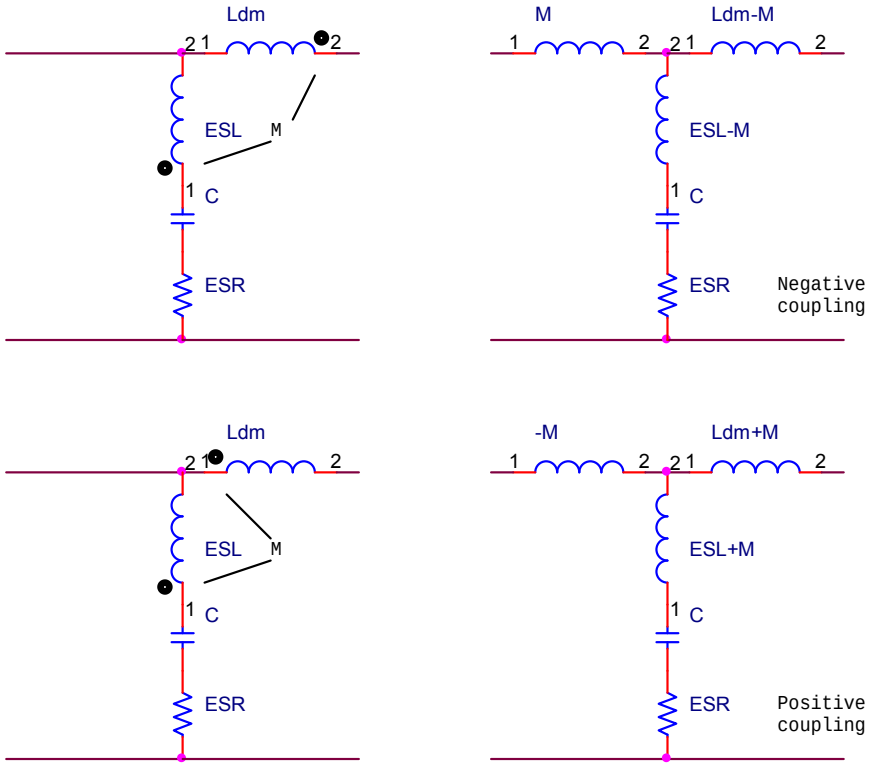


Fig. 3.9. Coupling between capacitor branch and CM choke

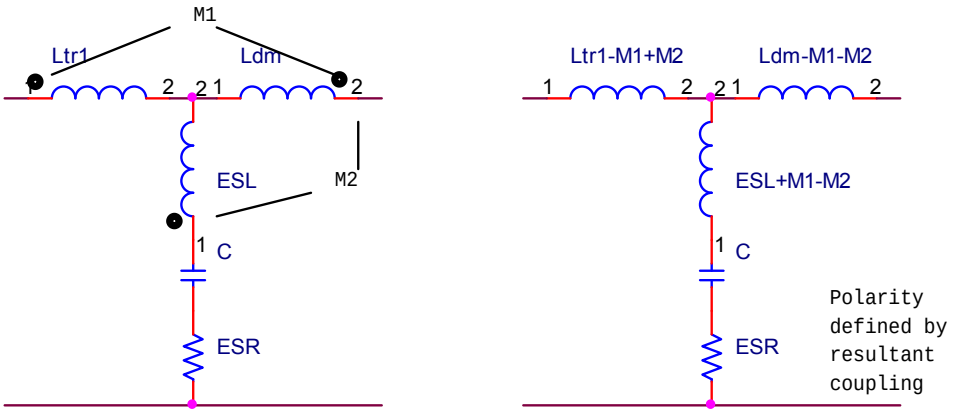


Fig. 3.10. Coupling between capacitor branch, input/output trace loop and CM choke

The impedance of capacitor is determined:

$$Z_{in} = j\omega \cdot ESL + ESR + \frac{1}{j\omega C} = ESR + j\left(\omega \cdot ESL - \frac{1}{\omega C}\right), \tag{3-5}$$

where ESR- capacitor equivalent series resistance,

ESL- capacitor equivalent series inductance.

The imaginary portion of equation (3-5) vanishes when:

$$\omega \cdot ESL - \frac{1}{\omega C} = 0 \ , \tag{3-6}$$

$$\omega = \frac{1}{\sqrt{ESL \cdot C}} = \omega_0 \ , \tag{3-7}$$

$$f_0 = \frac{1}{2\pi\sqrt{ESL \cdot C}} \ . \tag{3-8}$$

In equation (3-8) f_0 is commonly quoted as resonant frequency of a capacitor. It is possible to have a smooth transition between the capacitive region and inductive region for a capacitor. It is stated, that when the capacitor's equivalent series resistance is greater than or equal to the critical equivalent series resistance ESR_c, the transition is smooth [33].

The impedance of capacitor is determined by equation (3-5) and can be rewritten as second order differential equation.

$$Z_{in} = ESR + j\left(\omega \cdot ESL - \frac{1}{\omega C}\right) = \frac{\omega \cdot ESR \cdot C + j(\omega^2 \cdot ESL \cdot C - 1)}{\omega C}$$

$$= \frac{-\omega^2 + \frac{j\omega}{ESL} + \frac{1}{ESL \cdot C}}{\frac{ESR}{j\omega}} \ . \tag{3-9}$$

The solution for this equation consists of two parts: the complementary solution and particular solution. Complementary solution, which is solution of the homogenous differential equation in denominator- $-\omega^2 + \frac{j\omega}{\frac{ESL}{ESR}} + \frac{1}{ESL \cdot C}$ is also called a natural circuit response. Resonance frequency ω_0 can be directly written as:

$$\omega_0^2 = \frac{1}{ESR \cdot C} , \tag{3-10}$$

$$\omega_0 = \frac{1}{\sqrt{ESL \cdot C}} , \tag{3-11}$$

and Neper frequency, α as:

$$2\alpha = \frac{1}{\frac{ESL}{ESR}} , \tag{3-12}$$

$$\alpha = \frac{ESR}{2 \cdot ESL} . \tag{3-13}$$

The damping ratio, ζ, namely:

$$\zeta = \frac{\alpha}{\omega_0} = \frac{ESR}{2} \sqrt{\frac{C}{ESL}} . \tag{3-14}$$

If values of damping coefficient are greater than or equal to $1/\sqrt{2}$, there is no peak in the impedance curve:

$$ESR \geq \sqrt{2} \sqrt{\frac{ESL}{C}} . \tag{3-15}$$

And critical impedance can be approximated as:

$$ESR_c \approx 1.14 \sqrt{\frac{ESL}{C}} . \tag{3-16}$$

Capacitor branch impedance incorporating mutual inductance M can be stated using equation (3-17) for the positive coupling:

$$Z_1 = ESR + j\left(\omega \cdot (ESL + M) - \frac{1}{\omega C}\right) . \tag{3-17}$$

Thus, the resonance frequency:

$$f_1 = \frac{1}{2\pi\sqrt{(ESL + M)C}} . \tag{3-18}$$

Capacitor branch impedance incorporating mutual inductance M can be stated using equation (3-19) for the negative coupling:

$$Z_2 = ESR + j\left(\omega \cdot (ESL - M) - \frac{1}{\omega C}\right) . \quad (3\text{-}19)$$

Thus, the resonance frequency, if the ESL of capacitor is higher than mutual inductance, can be expressed:

$$f_2 = \frac{1}{2\pi\sqrt{(ESL - M)C}} . \quad (3\text{-}20)$$

In case if the mutual inductance is higher than ESR of capacitor, resonance frequency is:

$$f_3 = \frac{1}{2\pi\sqrt{(M - ESL)C}} . \quad (3\text{-}21)$$

Resonance frequency, in case of positive mutual coupling, f_1 is lower than the resonance frequency f_2 when negative mutual coupling exists, if the mutual inductance is lower than ESL of capacitor branch ($ESL > M$). Though, if ESL of capacitor branch is lower than mutual inductance in case of negative coupling ($ESL < M$), resonance frequency f_3 lays in between f_1 and f_2, therefore in this case no change of phase polarity occurs. It could be highlighted, when the negative coupling compensates the ESR of capacitor branch ($ESL = M$), no resonance and no change of phase polarity occur and impedance of capacitor can be simplified in equation (3-22):

$$Z_4 = ESR + j\left(\omega \cdot (ESL - M) - \frac{1}{\omega C}\right) = ESR - j\left(\frac{1}{\omega C}\right). \quad (3\text{-}22)$$

As it can be concluded from equation (3-22) the impedance in higher frequency region is strongly dependent only on capacitors branch ESR, as no inductance exists in this case. Capacitor for usage in EMC filters is limited by its resonance frequency and the rising of this parameter is of great importance.

There are plotted calculated examples of capacitor branch impedance magnitude and impedance angle, in Fig. 3.11. and Fig. 3.12, if C=0.61uF, ESR=0.08Ω, ESL=9.49nH.

It can be concluded, from the five plotted curves on Fig. 3.11., that the best high frequency performance offers the case, when the mutual coupling cancels the capacitor branch ESL. The worst high frequency performance can be expected, when the mutual coupling is much higher than capacitor branch ESR, no mater of coupling polarity and it's the worst case of the examined cases.

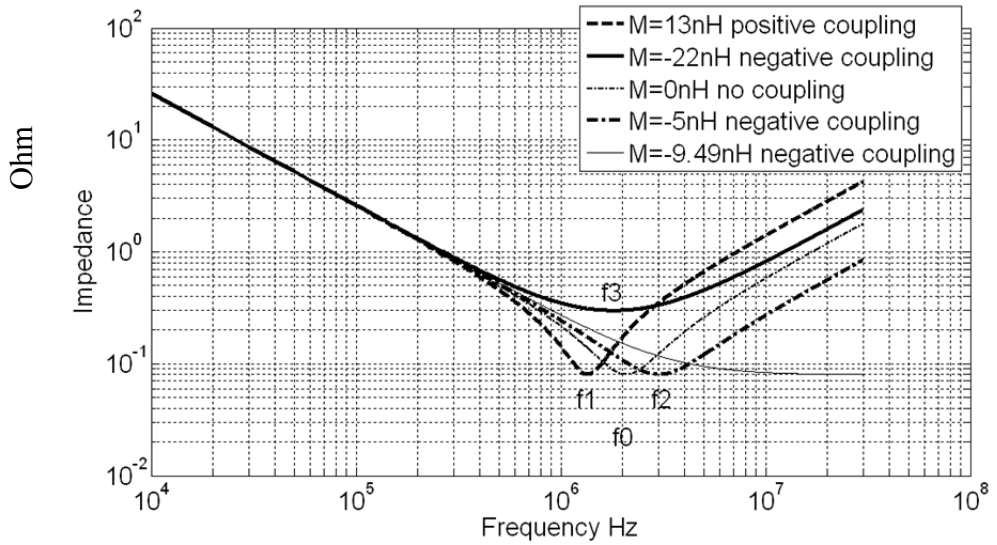


Fig. 3.11. Impedance of capacitor branch

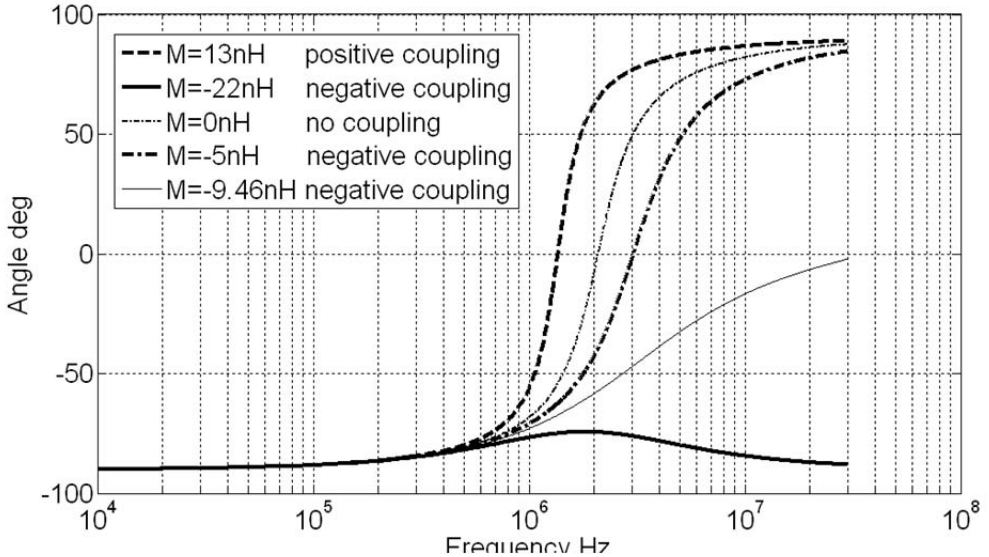


Fig. 3.12. Phase angle of capacitor branch

3.4 Extraction of mutual inductance between common mode choke and capacitor branch, input/output trace loops M2, M5 and M1, M4.

Mutual inductance parameters are extracted from 2-port network S-parameter measurements, which are made using vector network analyzer R&S ZVRE. As three-phase filter is not a 2-port network, it is modified to enable correct 2-port network measurements, as shown in Fig. 3.13, thus modifications leave negligible effect on filter DM performance. All three phase

filter component parasitic elements are extracted from 1-port S-parameter measurements converting them to Y and Z-parameters, using R&S ZVRE and it`s built in functions.

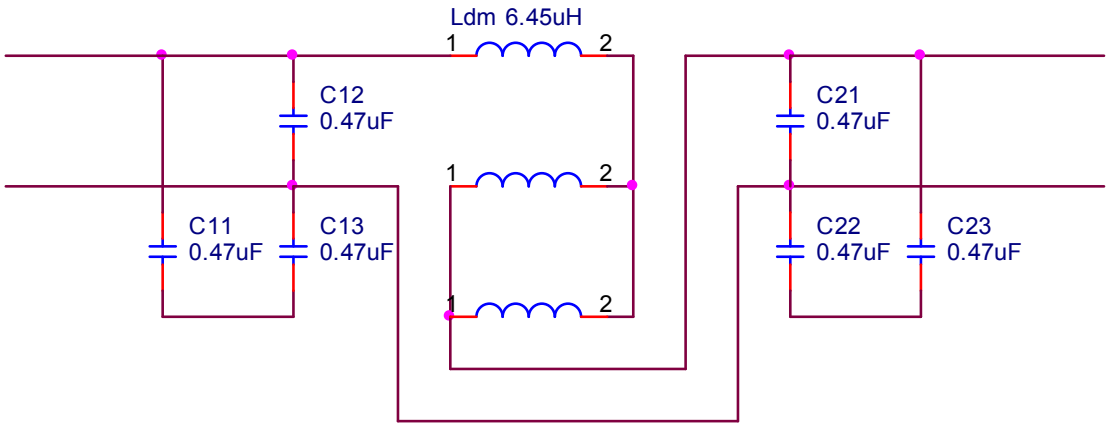


Fig. 3.13. Three phase filter modification to enable 2-port S-parameter measurements

The first, filter with horizontal CM choke is investigated. All couplings are defined in Fig. 3.6. For purposes of M2 extraction all other mutual inductances should be minimized or eliminated, thus on PCB only CM choke and C1 capacitor branch are left. Ltr1 and Ltr2 are minimized connecting the VNA directly to C1 capacitor branch and CM choke, so M4, M5, M6 are minimized. Capacitor branch C2 is dismounted to eliminate related mutual inductances- M1, M3. M2 is extracted from capacitor branch impedance.

To extract M5 inductive coupling VNA are connected to filter terminals next to Ltr1, thus Ltr1 inductance is incorporated in measured data as well as Ltr1 side effect- M5 mutual coupling. Capacitor branch impedances and angles with and without couplings are plotted on Fig. 3.14. Capacitor branch C1 impedance has a resonance at the point where the phase angle equals zero- f_{C1}=1.999MHz. Capacitor branch C1 impedance with coupling M2, as it can be seen on Fig. 3.14., does not have phase angle change at resonance (resonance at 17.58MHz are resonance connected to CM choke and parasitic capacitances, respectively it out of scope), thus resonance frequency of capacitor branch is defined by equation (3-21).

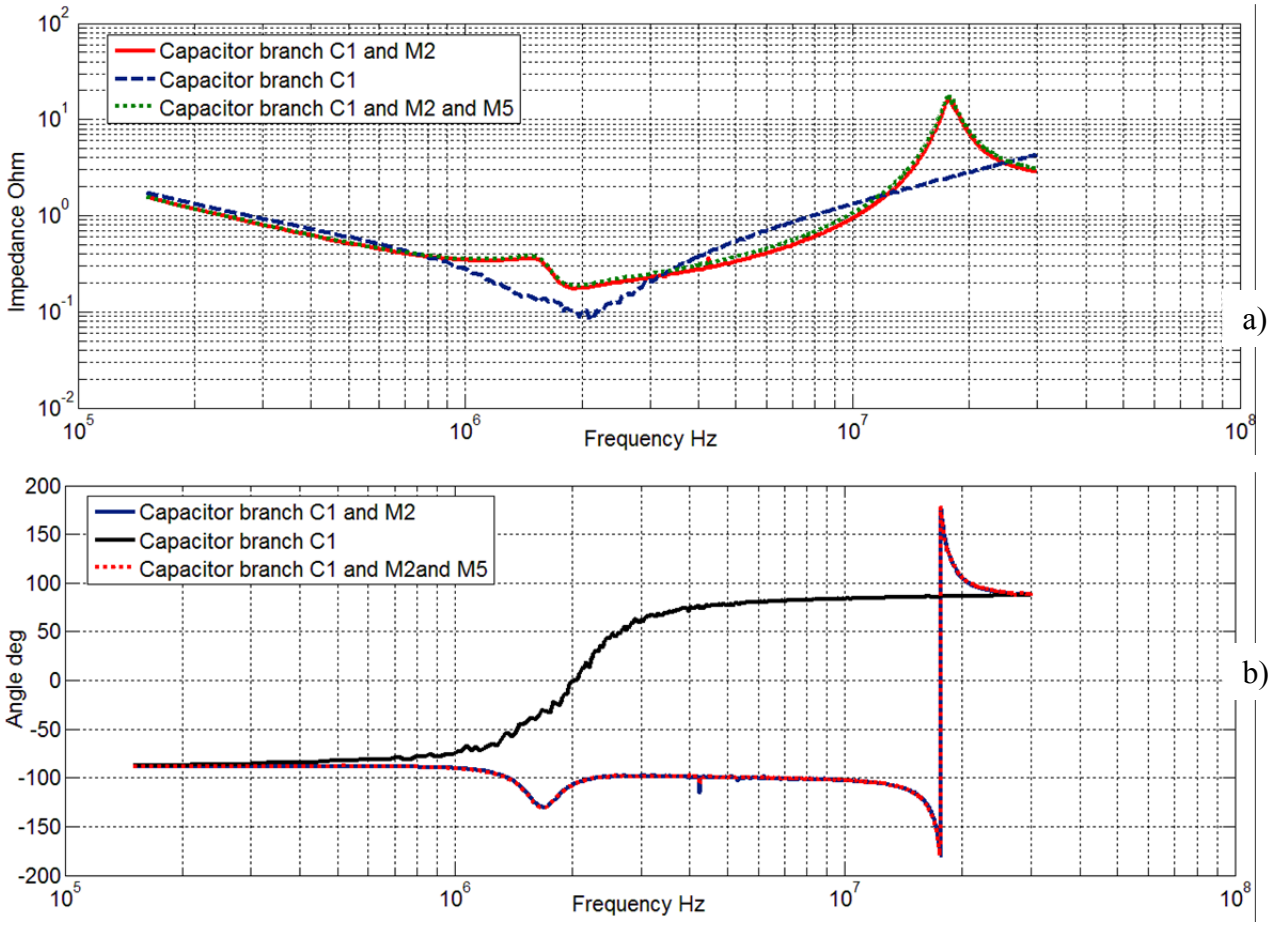


Fig. 3.14. Capacitor branch C1: a) impedance, b) phase with M2 and M5 inductive coupling

Resonance of capacitor C1 branch occurs at frequency f_{M2} =1.909MHz. Capacitor C1 branch with coupling M2 has no impedance phase angle change and M2 can be calculated using equation (3-23) derived from equation (3-21).

$$M_2 = \frac{1}{4\pi^2 f^2 C} + ESL. \tag{3-23}$$

Capacitor branch C1 impedance with couplings M2 and M5 does not have phase angle change at resonance frequency f_{M2M5} =1.969MHz, so the total effect of couplings M2 and M5 can be calculated using equation (3-23). Calculated mutual inductance M2=-21.55nH, total mutual inductance M2+M5=-20.88nH. Thus, mutual inductance M5=0.67nH is positive, but it's magnitude is small in respect to M2, so the total effect of couplings M2 and M5 on capacitor branch is negative.

The coupling polarity and magnitude strongly depends on the common mode choke construction (distribution of leakage inductance flux whose are responsible for DM inductance). There are no such possibilities of winding configurations for three phase common mode chokes

as for one phase common mode chokes [41], so here are examined two types of common mode chokes- horizontal and vertical placement configurations.

Three phase filter are made symmetrical visually, but since it is impossible to place the three phase CM choke symmetrically in respect to all capacitors, the filters mutual couplings M2, M5 and M1, M4 are not equal as it is in case of one phase filters and they should be calculated separately.

Extraction of mutual inductances M1 and M4 are done likewise M2 and M5 extraction. There are capacitor branch C2 and CM choke kept on PCB, so the mutual inductances M2 and M3 are eliminated.

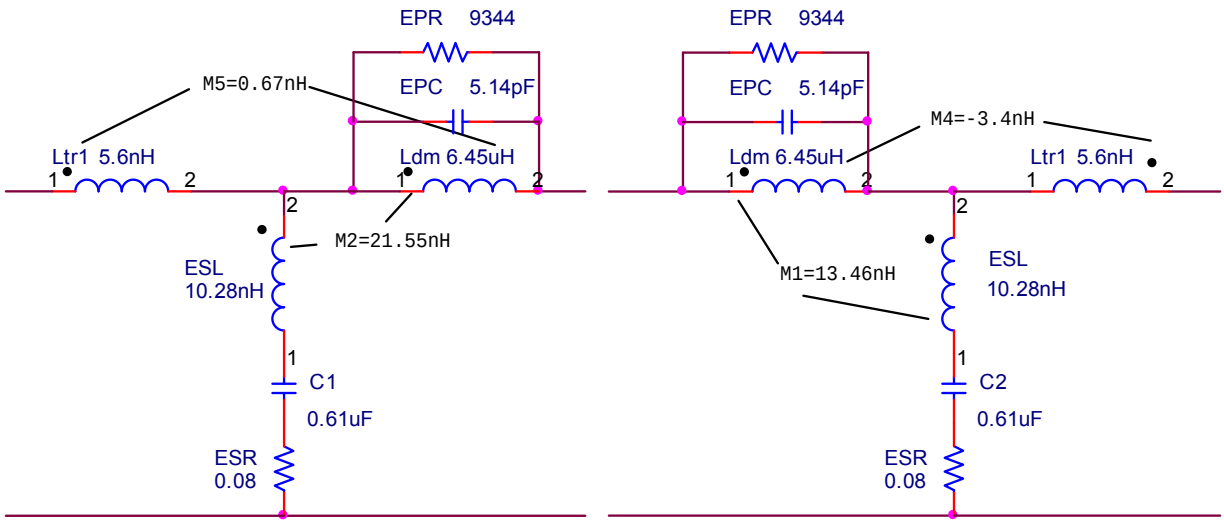


Fig. 3.15. Capacitor C1 branch with M2 and M3 inductive coupling and capacitor C2 branch with M1 and M4

Ltr1 and Ltr2 are minimized connecting the VNA directly to C2 capacitor branch and CM choke, so M4, M5, M6 are minimized. M1 is extracted from capacitor C2 branch.

To extract M4 inductive coupling VNA are connected to filter terminals next to Ltr2, thus Ltr2 inductance is incorporated in measured data as well as Ltr2 side effect- M4 inductive coupling. Capacitor branch impedances and angles with and without couplings are plotted on Fig. 3.16.

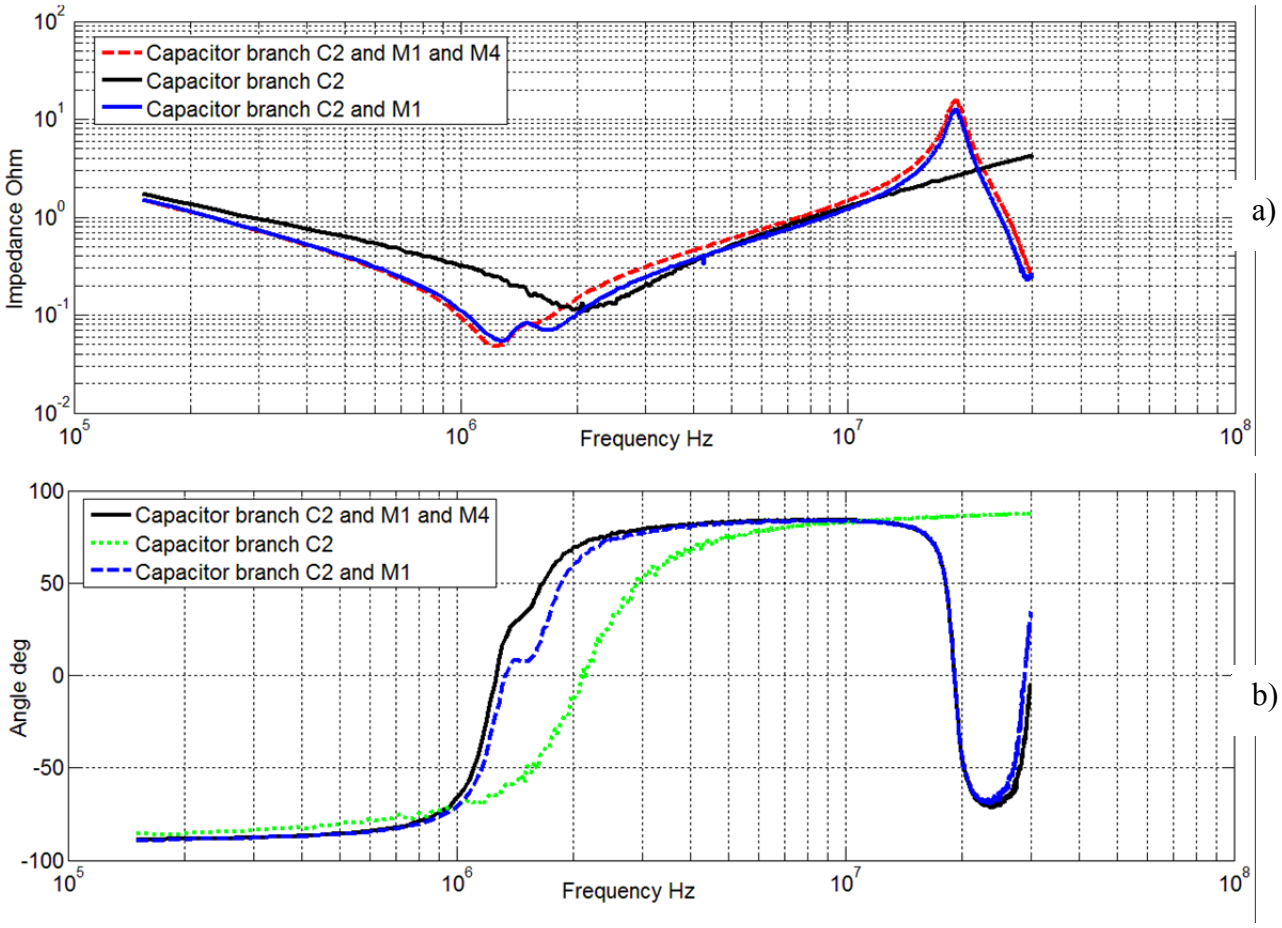


Fig. 3.16. Capacitor C2 branch: a) impedance, b) impedance angle with M1 and M4 inductive coupling

Capacitor branch C2 impedance has a resonance at the point where the phase angle equals zero- f_{C1}=2.088MHz. Capacitor branch impedance with and without mutual couplings M1 and M4 can be seen at Fig. 3.16.

The resonance of capacitor branch incorporating M1 and M1, M4 are f_{M1}=1.343MHz, f_{M1M5}=1.253MHz. Both couplings are positive, because of resonance frequencies $f_{C1}>f_{M1}>f_{M1M5}$, thus couplings can be calculated modifying equation (3-18):

$$M_1 = \frac{1}{4\pi^2 f^2 C} - ESL \ . \tag{3-24}$$

Calculated mutual couplings are: M1=13.46nH and M4=3.4nH.

In the same manner three phase filter mutual inductances are extracted when horizontal CM choke is replaced with vertical CM choke, while capacitors are left the same. Mutual coupling between input output trace loops and CM choke and capacitor branches C1, C2 and CM choke are strongly influenced. Results are collected in Table 3.1.

Table 3.1.

Mutual inductance magnitude, depending on CM choke construction

CM choke type	M2	M5	M1	M4
Horizontal	-21.55nH	0.76nH	13.46nH	3.4nH
Vertical	32.55nH	0.58nH	18.99nH	0.84nH

Vertical alignment of CM choke and winding construction leads to positive coupling between CM choke and capacitor branch unlike it is in case of horizontal CM choke, either magnitude increases.

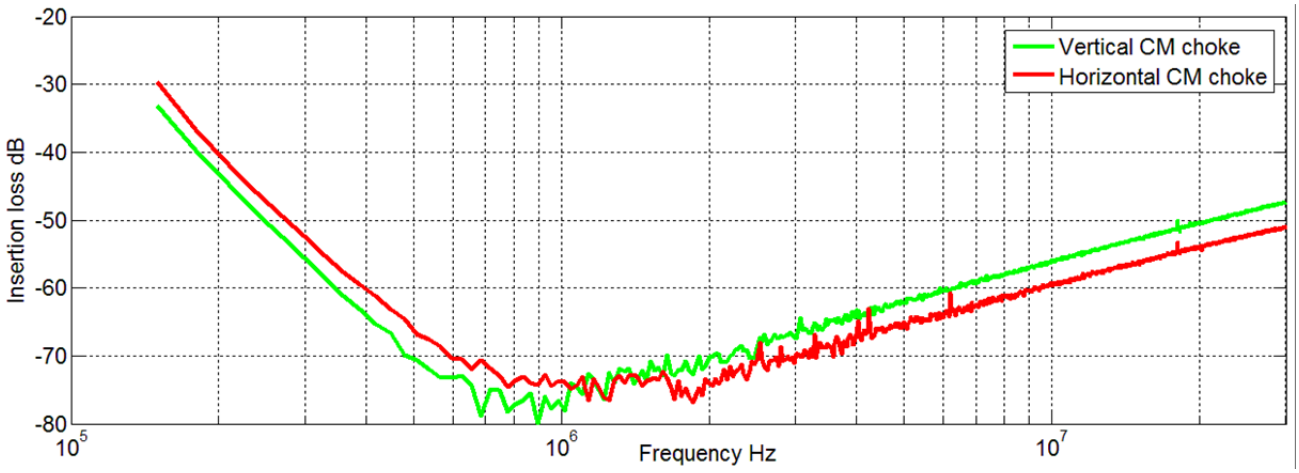


Fig. 3.17. Three phase filter insertion loss

In case of vertical CM choke mutual inductance between CM choke and input/output trace loops decreases.

To show the importance of CM choke construction measured S-parameters are converted to forward insertion gain, whose are compared in Fig. 3.17. Low frequency gain of three phase filter with vertical CM choke construction is ~4dB better than three phase filter with horizontal choke, but high frequency range filter with horizontal alignment of CM choke have ~4dB advantage in comparison to filter with vertical CM choke.

3.5 Extraction of mutual inductance between capacitor branches

Mutual coupling exists between capacitor branches due to capacitors equivalent series inductance ESL. Usually engineers in filter design don't take into account mutual coupling between closely positioned capacitors. One of the capacitor branches bypasses the disturbance current, so the other capacitor branch is a low current loop, on witch mutual coupling has large

impact. Three phase filter is modified as a two pole network, as in Fig. 3.13. In the Fig. 3.18.a situation is displayed for M3 extraction. To eliminate and minimize other parasitics and mutual couplings the trace loops Ltr1 and Ltr2 are minimized, thus M4, M5, M6 are eliminated, the CM choke are removed from PCB, thus M1, M2, M7, C_p are eliminated. The coupling M3 represents total mutual coupling between the capacitor branch C1 consisting of C11, C12, C13 and capacitor branch C2 consisting of C21, C22, C23 as displayed in Fig. 3.6. Taking into account the equivalent coupling polarities the capacitor branch C1 and C2 equivalent circuit are developed in Fig. 3.18.b, where the coupling are replaced with equivalent circuit. Using S-parameter measurement technique and converting measurements to T-network the M3 impedance can be calculated [45].

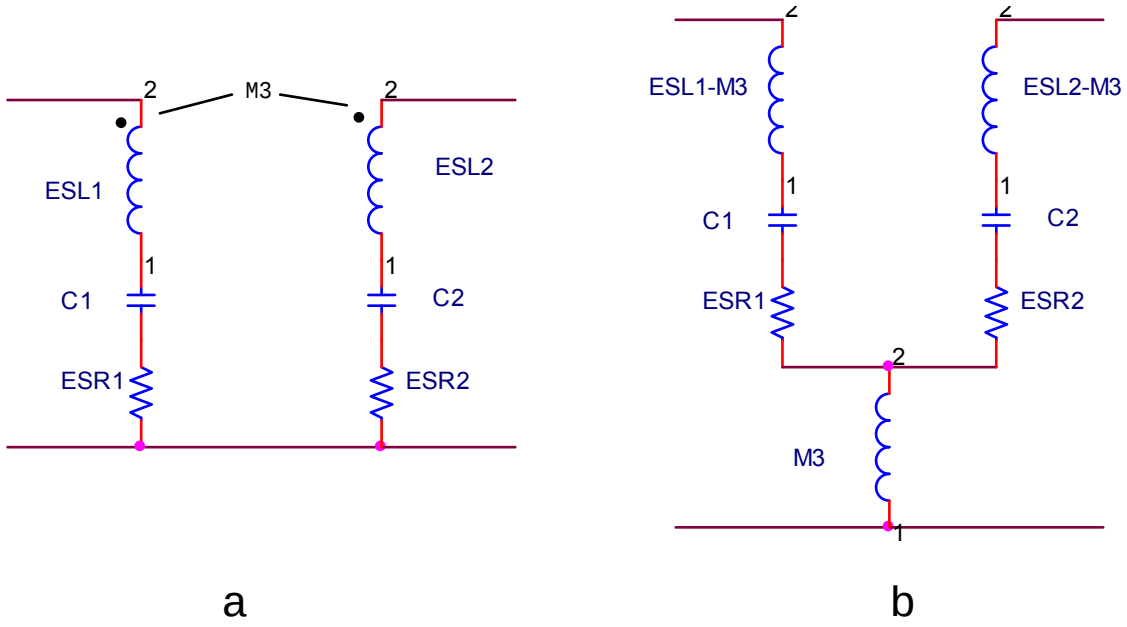


Fig. 3.18. a) Mutual inductance between capacitor branches, b) Equivalent circuit of mutual inductance between capacitor branches

The mutual coupling M6 is extracted in the same manner. To eliminate and minimize other parasitics and mutual couplings the CM choke are removed from PCB, thus M1, M2, M4, M5, M7, C_p are eliminated. Taking into account the equivalent coupling polarities the capacitor branch C1 and C2, input output trace loop Ltr1 and Ltr2 equivalent circuit are developed in Fig. 3.19.b, where the couplings are replaced with equivalent circuit. Using S-parameter measurement technique and converting measurements to T-network the total impedance of M3 and M6 can be calculated, afterwards, mutual coupling M6 can be calculated separately.

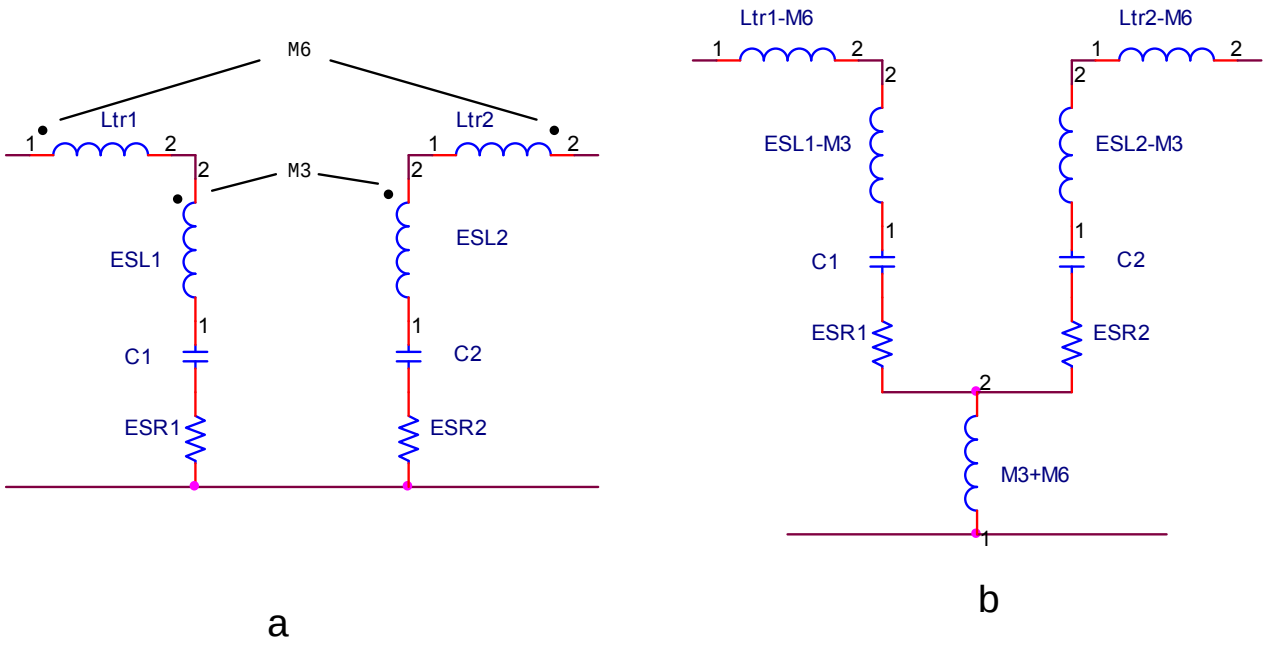


Fig. 3.19. a) Mutual inductance between capacitor branches and input output trace loops, b) Equivalent circuit of mutual inductance between capacitor branches and input output trace loops

The calculated results of mutual coupling magnitude of impedance and impedance angle are represented on Fig. 3.20. Measured data up to 500kHz are invalid doe to high noise floor of vector network analyzer. Calculated mutual couplings are M3=0.39nH and M6=0.14nH.

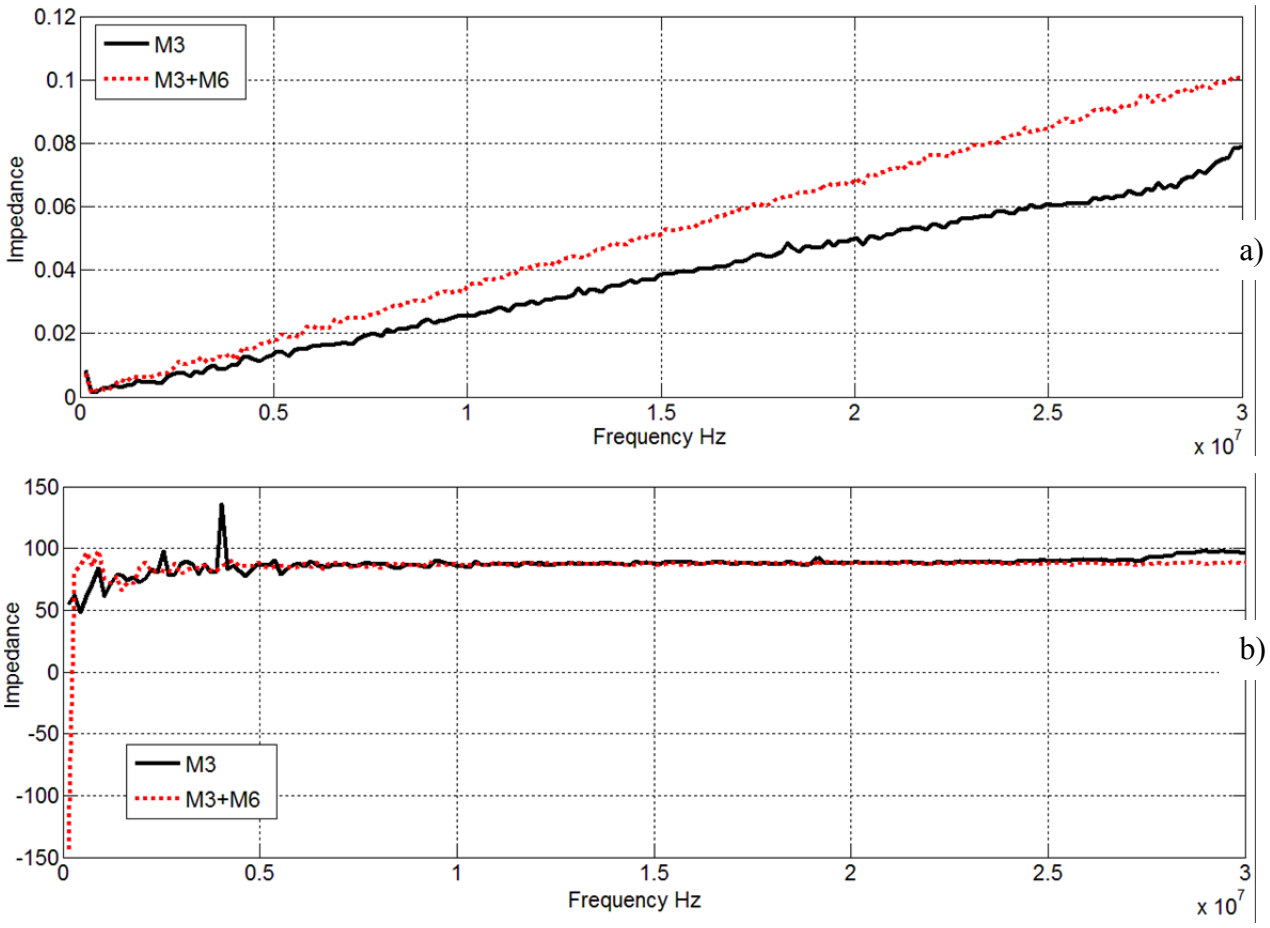


Fig. 3.20. Mutual coupling impedance a) Magnitude, b) angle

3.6 Ground plane created mutual inductance M7 and coupling capacitance Cp

Ground plane and input output trace loops are creating capacitive coupling Cp. Capacitance Cp can be divided in series of coupling capacitances between input and output traces, input and ground plane, output and ground plane. The main contribution on mutual coupling between input and output are delivered by mutual capacitance between traces and ground Cp1-Cp6, because of large area between them and close proximity, depending on PCB thickness. Mutual capacitances parallel to CM choke Cp7, Cp8, Cp9 have negligible impact on Cp, but it can be considered important when ground plane are between the traces on the same PCB layer. Dispersed coupling capacitances are shown on Fig. 3.21., where they are displayed on three phase filter top and side views.

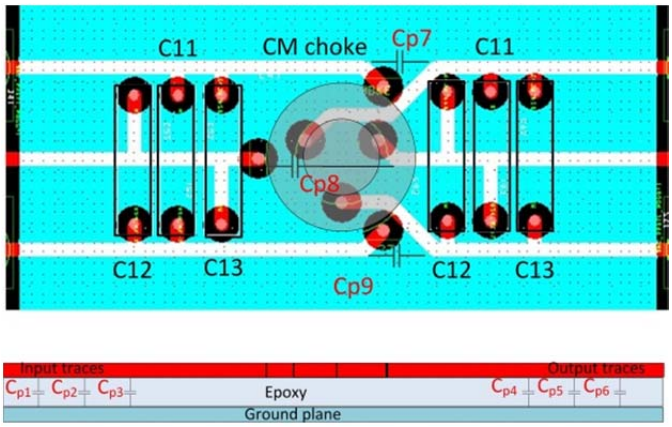


Fig. 3.21. PCB of three phase filter top and side view

Mutual coupling Cp represents total coupling of parasitics in parallel with CM choke equivalent parasitic capacitance- EPC. For high frequency noise, coupling Cp and parasitic capacitance of CM choke creates a high frequency shortcut between input and output, lowering the filters performance.

Coupling M7 is CM choke coupling to ground plane- the leakage flux created eddy currents in ground plane of PCB. This coupling is extracted using s-parameter measurements. CM choke DM impedance is measured, when the CM choke is not mounted on PCB and when the choke is mounted on PCB. The circuit for s-parameter measurements is the same as in Fig. 3.13. To eliminate all other mutual couplings capacitor branches are not mounted on PCB, eliminating mutual couplings M1, M2, M3, M4, M5, input output trace loops are minimized connecting VNA next to CM choke, thus M6 is minimized to negligible value. All impedances of CM choke horizontal alignment are shown in Fig. 3.22.

Measured impedances have various resonance frequencies. Thus, impedance resonance frequency of horizontal CM choke when mounted on PCB is: f_{PCB}=1.91MHz, but horizontal CM choke impedance resonance frequency measured alone is: f_{CM}=2.764MHz.

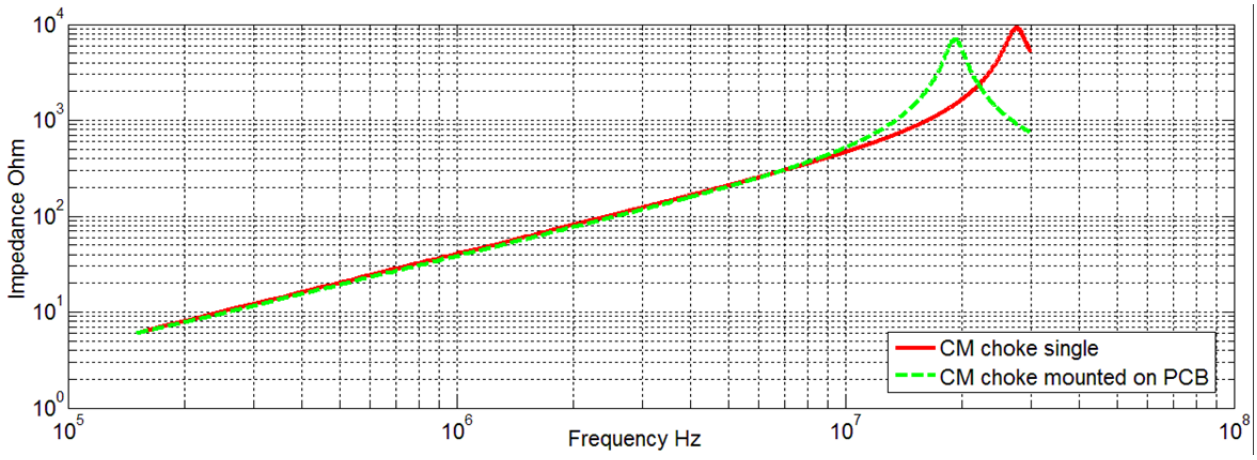


Fig. 3.22. Impedance of horizontally mounted CM choke

As can be concluded the mutual inductances and coupling capacitances created by PCB configuration decrease the horizontal CM choke performance, thus decreasing high frequency performance of the filter. Impedances of horizontal CM choke are calculated using equation (3-25) using measured S-parameters:

$$Z_{L_{CM}} = 2Z_0\left(\frac{1}{S_{21}} - 1\right), \tag{3-25}$$

where, Z_0=50Ω characteristic impedance of analyzer.

Inductances of horizontal CM choke are calculated using linear part of curve up to 10MHz using (3-26). The parasitic capacitance of horizontal CM choke- EPC, are calculated using equation (3-27).

$$L = \frac{Z_{lin}}{2\pi f_{lin}}, \tag{3-26}$$

$$EPC = \frac{1}{(2\pi f_0)^2 L}, \tag{3-27}$$

where Z_{lin} and f_{lin} are impedance and frequency in the linear region of horizontal CM choke impedance and f_0 is impedance resonance frequency.

When horizontal CM choke is measured alone the calculated inductance is 6.45uF and parasitic capacitance 5.14pF. When horizontal CM choke is mounted on PCB inductance decreases to 6.14uH and parasitic capacitance increases to 11.28pF. Mutual inductance M_7=0.31uH, the difference between two inductances, thus M_7 leads to reduction of horizontal CM choke differential mode inductance- horizontal CM choke leakage inductance. Parasitic capacitance created by PCB construction is: C_p=6.14pF, the difference between two calculated capacitances.

In the same manner parameters of vertical CM choke are calculated using the obtained measurement data shown in Fig. 3.22.

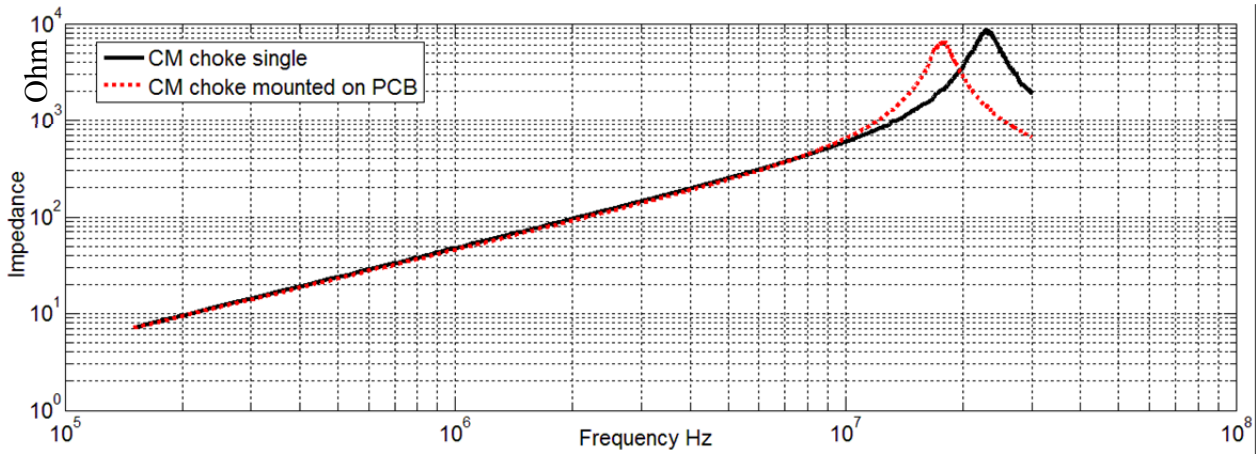


Fig. 3.23. Impedance of vertically mounted CM choke

Thus, impedance resonance frequency of vertical CM choke when mounted on PCB is: f_{PCB}=1.77MHz, but vertical CM choke impedance resonance frequency measured alone is: f_{CM}=2.30MHz. When vertical CM choke is measured alone the calculated inductance is 7.67uH and parasitic capacitance 6.23pF. When vertical CM choke is mounted on PCB inductance decreases to 7.63uH and parasitic capacitance increases to 10pF. Mutual inductance M_7=0.04uH, the difference between two inductances, thus M_7 leads to reduction of vertical CM choke differential mode inductance- vertical CM choke leakage inductance. Parasitic capacitance created by PCB construction is: C_p=3.77pF, the difference between two calculated capacitances. Data on vertical and horizontal CM choke are grouped in Table 3.2.

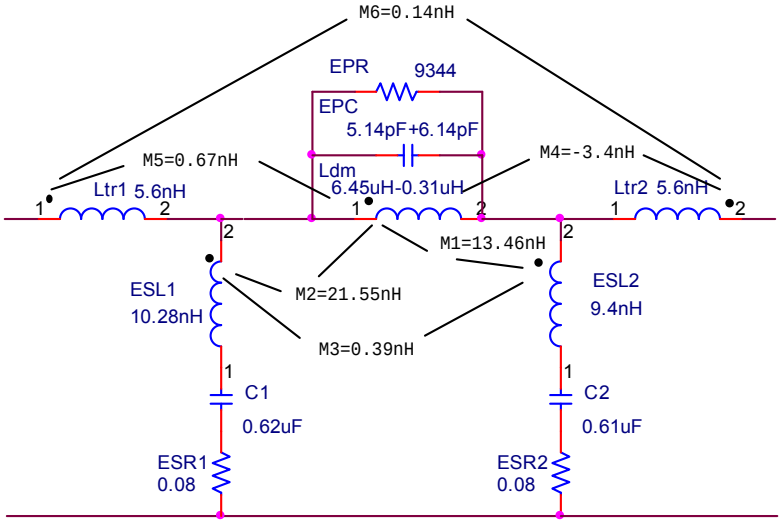
Table 3.2.

Vertical and horizontal CM choke parameters

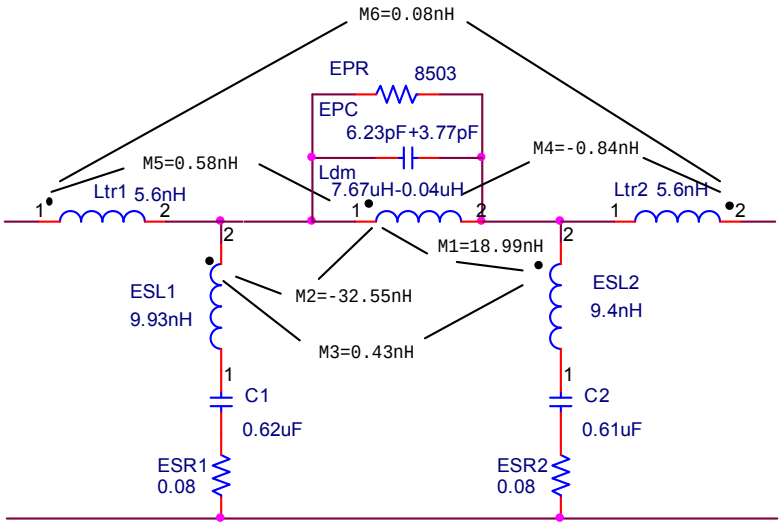
CM choke type	f_{PCB}	f_{CM}	M7	C_p	L
Horizontal	2.76MHz	1.91MHz	0.31uH	6.14pF	6.45uH
Vertical	2.30MHz	1.77MHz	0.04uH	3.77pF	7.67uH

3.7 One phase differential mode model of three phase filter

Using data from previous sub-chapters, DM model of three phase filter one phase can be built and verified. Model is built and simulated in PSpace, using all extracted mutual inductances, capacitive couplings and self parasitics of filter components.



a



b

Fig. 3.24. Extracted DM models of three phase filter one phase: a) Horizontal CM choke alignment; b) vertical CM choke alignment

Created model can be used to explore all relevant parasitic parameters that are critical for filter performance and parasitic parameters that have negligible effect on filter performance. Created model is verified using measured gain of the filter. Gain measurements are made using

R&S vector network analyzer ZVRE, thus 50Ω measurement system is used. Also the modeling is done using 50Ω characteristic system impedance. Models of filters with vertical and horizontal CM choke alignment, with component self parasitics and mutual inductances, parasitic capacitances are shown on Fig. 3.24.

It should be noted that positive and negative coupling of mutual inductances is not defined only by mutual inductance sign. The dots next to the inductance symbol in model schematic also should be taken into account.

Measured gain and simulated gain of both filters are displayed in Fig. 3.25. and Fig. 3.26.

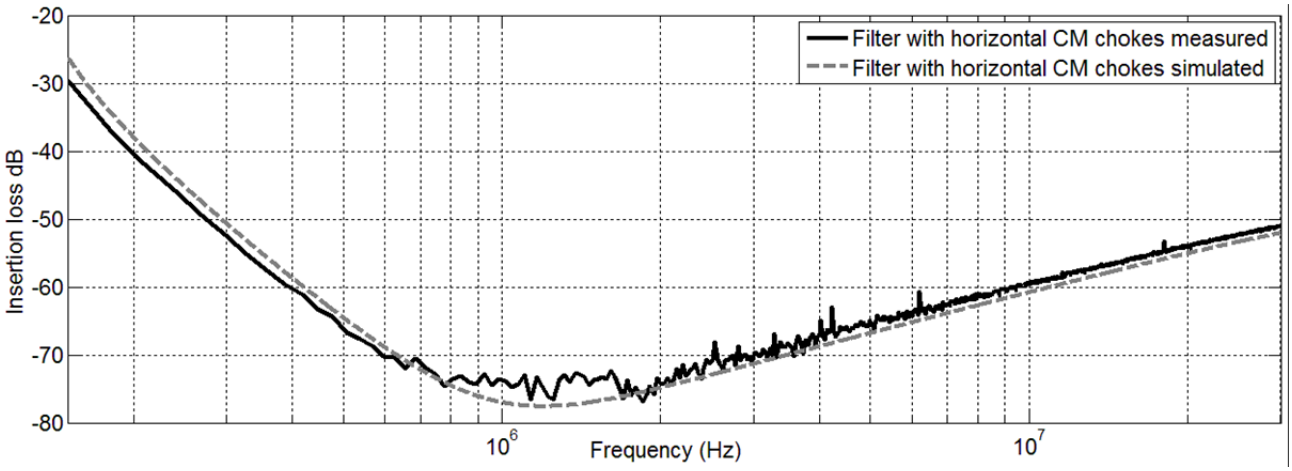


Fig. 3.25. Three phase filter with horizontal CM choke one phase insertion loss

Simulated and measured gains of both filters match very closely, so, the created models of three phase filter one of the phases are valid. Also the extraction procedures of mutual inductances and capacitive couplings are valid for three phase filter, equally as for one phase filters as it is described in previous subsections based on [41] and [45].

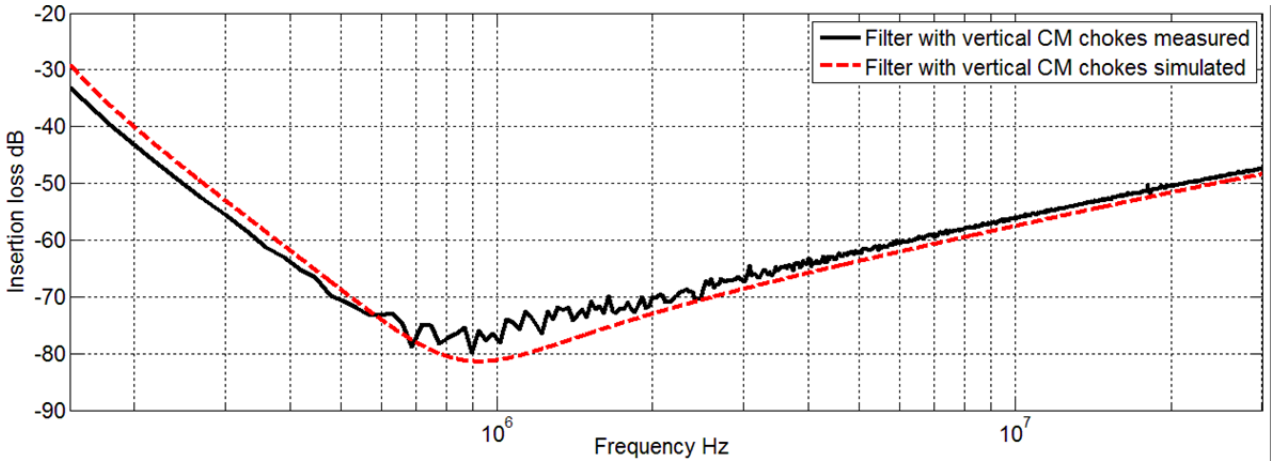


Fig. 3.26. Three phase filter with vertical CM choke one phase insertion loss

3.8 Analysis of mutual couplings in three phase filter

To realize the most important coupling mechanisms that distort high frequency insertion loss of three phase filters, mutual couplings are divided in three groups:

1) Couplings between capacitor branches and CM choke (M1, M2),
2) Couplings created by PCB and component interaction (M4, M5, M6, M7, Cp),
3) Coupling between two capacitor branches (M3).

Analysis is done using created models in Pspice. For simulations, model of filter with vertical CM choke is chosen.

3.8.1 Mutual couplings between common mode choke and capacitor

Mutual couplings created by CM choke and capacitor branches C1 and C2 are M1 and M2, respectively. The couplings are created by capacitors parasitic element ESL and CM choke leakage inductance L_{dm}. To show the impact of these couplings, multiple simulations are done and results are shown in Fig. 3.27. As reference there are simulated filter with all mutual couplings as in Fig. 3.26.

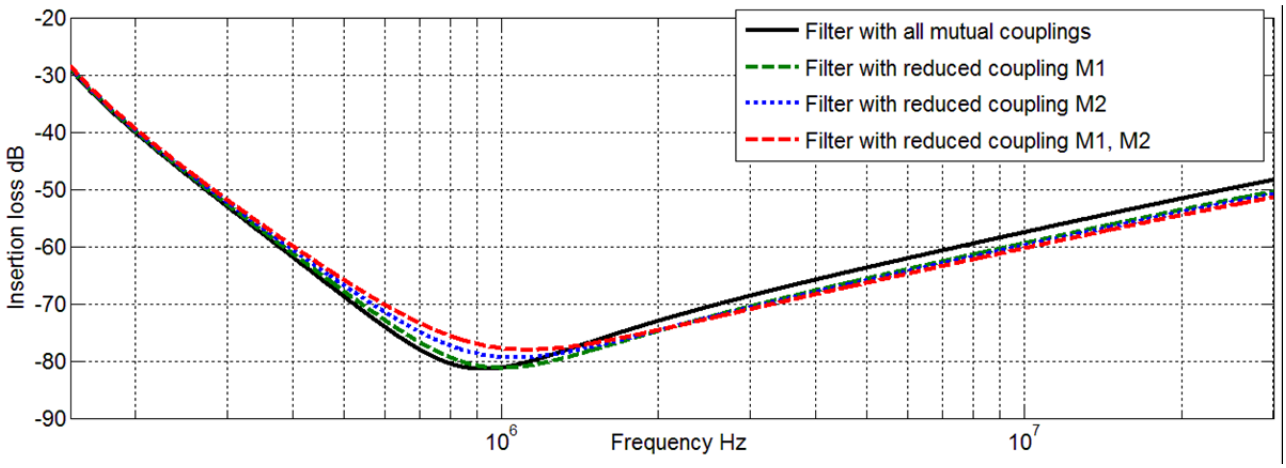


Fig. 3.27. Filter insertion loss, affected by mutual couplings, created by CM choke and capacitors

3.8.2 Mutual couplings created by PCB and component interaction

PCB interaction with components mounted on it, creates bunch of couplings- M4, M5, M6, M7 and Cp. To show the importance of these couplings, multiple simulations are done and results are shown in Fig. 3.28.

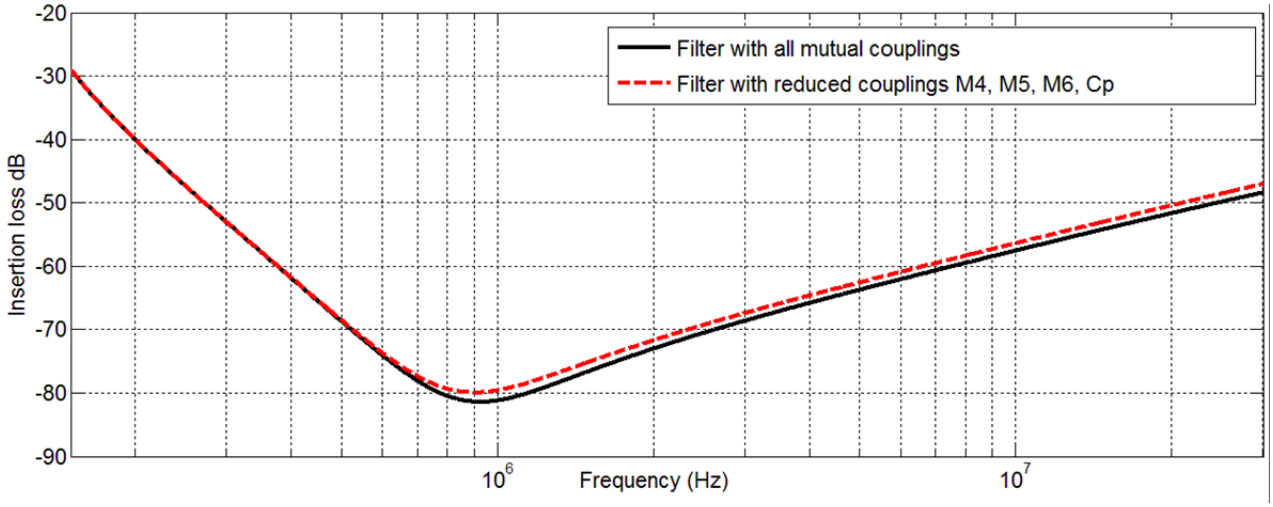


Fig. 3.28. Filter insertion loss, affected by mutual couplings, created by PCB interaction with components mounted on it

As reference there are simulated filter with all mutual couplings as in Fig. 3.26. Actually, reduction of couplings M4, M5 and Cp, created by PCB, leaves negligible effect on filters insertion loss, so they are not analyzed separately in Fig. 3.28. Reduction of couplings M4, M5,

M6, Cp decreases filter insertion loss in frequency range 0.8MHz. In fact, reduction of insertion loss is due to M6 reduction.

3.8.3 Mutual Coupling Created Between Capacitor Branches

Capacitor branches create mutual coupling M3, because of capacitors parasitic element-ESL. Importance of coupling M3 is shown in Fig. 3.29. Coupling M3 predominates over other mutual couplings. Reduction of M3 improves filter insertion loss in frequency range over 0.6 MHz more than 10 dB. However, previous analysis of other mutual couplings showed that they have little or negligible effect on filter insertion loss, therefore, if dominant coupling M3 is reduced, reduction of M1, M2, M4, M5, M6 and Cp improves filters insertion loss as it can be seen in Fig. 3.29. Ideal filter with no couplings and no component parasitics, except CM choke differential mode inductance L_{dm}, are shown in Fig. 3.29., as a reference.

To experimentally confirm mutual coupling M3 importance and dominance, measurement of insertion loss is done and shown in Fig. 3.30., if the CM choke is disconnected from PCB, but isolated and left on it, thus M1, M2, M4, M5, M7 and Cp are eliminated and in measurements only effect of mutual couplings M3 and M6 will appear.

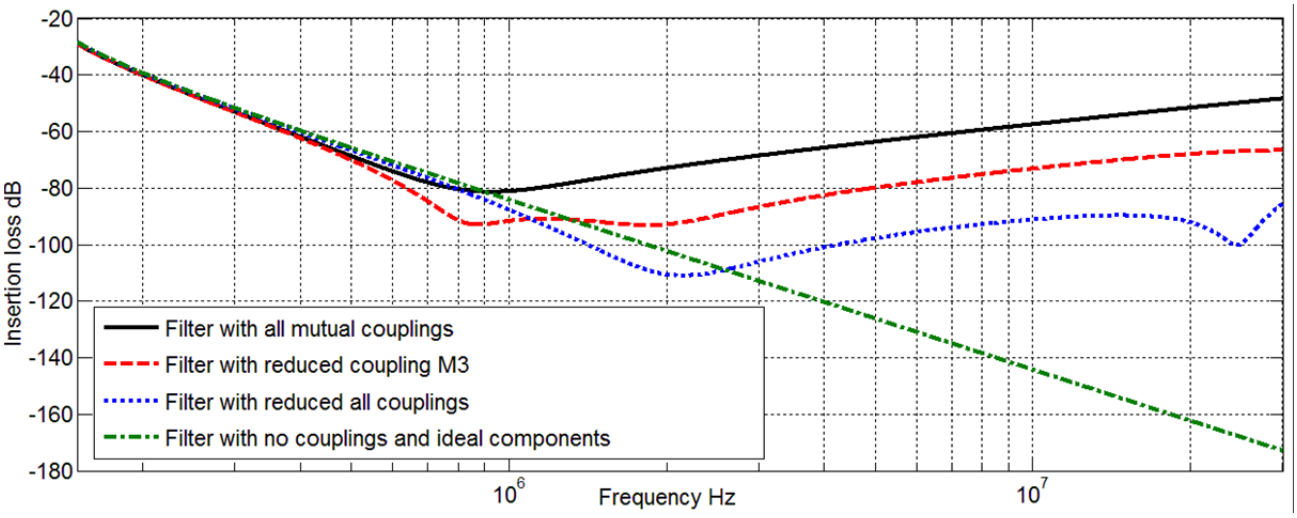


Fig. 3.29. Filter insertion loss, affected by mutual couplings and filter component parasitic elements

To eliminate coupling M6, test probes are connected directly to capacitor branches, thus avoiding inductive traces L_{tr1}, L_{tr2} and their coupling M6.

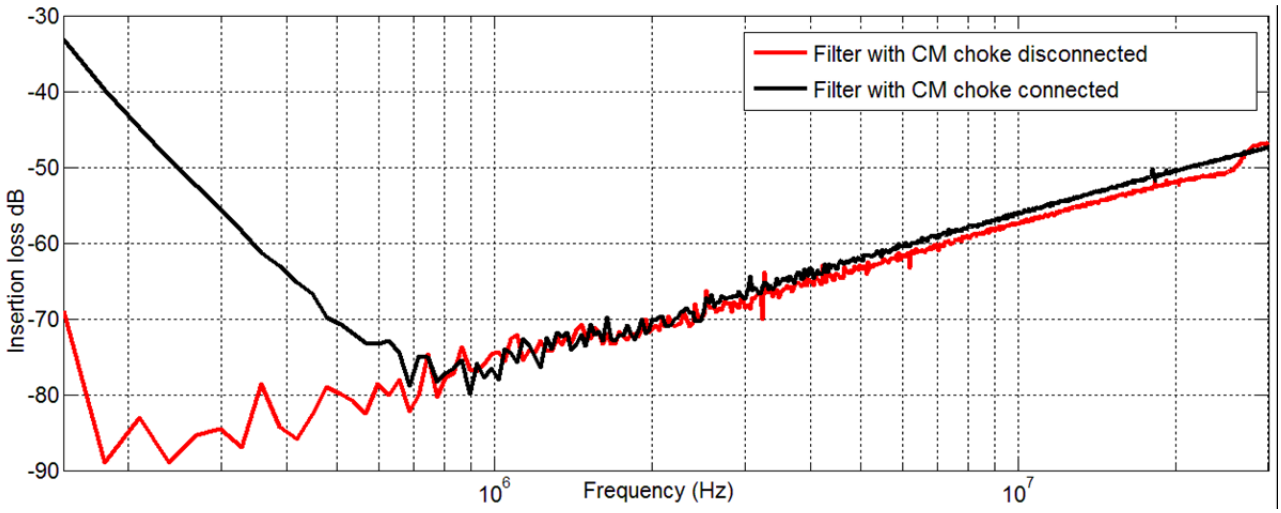


Fig. 3.30. Filter insertion loss with and without removed CM choke

CM choke have almost no impact on insertion loss in frequency range over 0.7 MHz. High frequency disturbances are passing thru more efficient path- M3, respectively.

3.9 Conclusions

Common mode choke alignment (vertical or horizontal) have an influence on mutual couplings M1, M2, M4 and M5. Horizontal placement of CM choke leads to negative mutual coupling on capacitor branch C1, but the magnitudes of coupling are similar, except M4 that reduces drastically in case of vertical alignment of CM choke. These two types of CM chokes have an impact on filter gain by approximately 4dB as it can be seen in Fig. 3.17.

Mutual inductance M7 reduces the leakage inductance of CM choke. Magnitude of M7 is affected mainly by CM choke placement above solid ground plane on PCB or other conductive surface in close proximity. Vertically positioned CM choke above PCB ground plane has larger leakage inductance (mutual inductance M7 is negligible) in comparison to horizontally positioned CM choke when part of the leakage flux is creating eddy current in PCB ground plane (mutual inductance M7 affects CM choke DM impedance.

Mutual inductance M7 reduces the leakage inductance of CM choke. Magnitude of M7 is affected mainly by CM choke placement above solid ground plane on PCB or other conductive surfaces in close proximity.

Common mode choke alignment (vertical or horizontal) have an influence on mutual couplings M1, M2, M4 and M5 however, impact on filters insertion loss is quite low if comparisons are made with CM choke impact on one phase filters in [41].

Mutual inductance M3 incorporating capacitor branches C1 and C2 creates shortcut for high frequency disturbance, and dominates over other mutual couplings worsening insertion loss, therefore it should be considered critical and should be terminated at the first point, when insertion loss improvement of filter should be obtained. Reduction of mutual coupling M3 improves filter insertion loss in frequency range over 0.6 MHz by more than 10dB.

Other mutual couplings have poor effect on insertion loss, but if they all are reduced simultaneously, insertion loss is improved by more than 10dB in frequency range over 2 MHz.

4. EFFECTS OF PARASITIC PARAMETERS ON THREE PHASE T TYPE EMI FILTER

4.1 Background

To achieve compliance with EMC conducted emission limit lines, usually filter with one common mode choke is used with couple of Y-capacitors for CM noise mitigation. Since, three phase CM chokes are the most expensive filtering components in EMI filters, two and more CM chokes are used rarely. Instead of CM chokes Y-capacitors are used. The value of the Y-capacitor is restricted by the permissible leakage current allowed [46] and [47]. The maximum leakage current is governed by standards and regulations and depends upon the type of equipment. It leads to necessity, to use two or more CM chokes, creating two stage filter or filter with more stages.

This chapter is devoted to investigation of T type three phase power electronic filter, shown in Fig. 4.1., layout related problems created by parasitics between filter components and self-parasitic elements of PCB. It will be shown that these parasitics have a serious influence on three phase filter insertion loss and that filter with identical components and identical topology can exhibit different performance in disturbance attenuation due to layout of PCB. Research will be done based on real three phase filer prototypes, from a real circuit standpoint so that results and conclusions can be transferred to many practical problems associated with three phase filter component placement and PCB layout considerations.

The investigation will be done on four type coupling effects, similarly classified as for one phase filters in [41]:

- mutual inductance between common mode choke and capacitor branch,
- mutual inductance between two common mode chokes,
- mutual inductance between common mode choke and PCB ground layer,
- coupling capacitance between PCB traces.

Other couplings analyzed in previous sections are neglected due to their negligible effect on filter insertion loss. Input-output trace loop mutual inductance in comparison to mutual inductance between two CM chokes is very low, therefore it is reasonable to ignore it due to model simplicity.

4.2 Three phase T type filter parasitic couplings

Three phase T type filter for power electronic EMC problem mitigation are shown in Fig. 4.1. Capacitor branch C1 consists of capacitors C11 C12 C13. They are used for DM disturbance attenuation, the capacitance is 0.47uF. CM chokes L1 and L2 are used for CM disturbance mitigation. Two type CM chokes are used. CM inductance of a three phase CM choke is the inductance of its three coils connected in parallel, but differential mode (DM) inductance is measured as defined in [43], [9] when two of the coils connected in paralel and the third is connected in series. Inductance for DM and CM part of chokes are different for both type of chokes. CM inductance L_{cm} of chokes is in range 0.20mH to 0.23mH and leakage inductance L_{dm} is in range 6.88uH to 6.94uH. More detailed inductances are defined in Fig. 4.1.

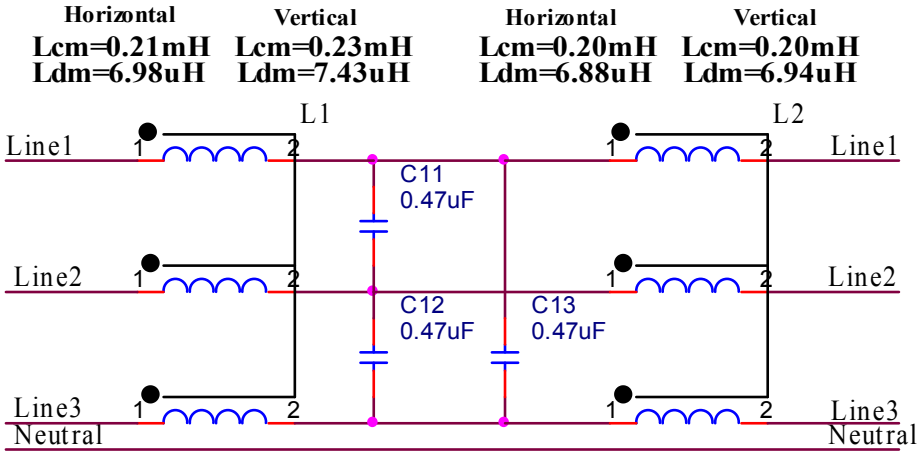


Fig. 4.1. Three phase T type filter prototype schematic

Two filter prototypes are shown in Fig. 4.2., with vertical CM chokes and horizontal CM chokes. Both filters have the same capacitors and PCB layouts. PCB contains two layers. The top layer is used as ground plane and bottom layer is used for component routing.

DM model is proposed for filters in Fig. 4.3.a and Fig. 4.3.b. similarly as in [15], [48]. As there are three phases in filter, three models should be estimated for one filter (Line1-Line2, Line2-Line3, Line 1-Line3). DM model parasitics are changing phase to phase. For sake of simplicity only the worst case model is presented- phase pair Line1- Line2 that during measurements has shown the higher mutual couplings.

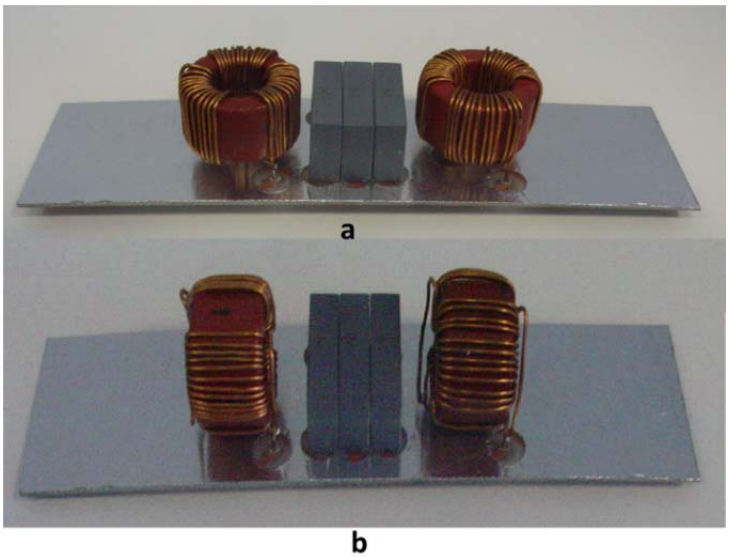


Fig. 4.2. (a Filter prototype with horizontal CM chokes, b) Filter prototype with vertical CM chokes

Five couplings are considered for current three phase T type filter:

- M3- inductive coupling between CM chokes,
- M1, M2- inductive coupling between CM chokes and capacitors,
- M4, M5- inductive coupling between CM chokes and PCB ground plane,
- C_{p1}, C_{p2}, C_{p3}- capacitive coupling between PCB input and output traces.

Mutual inductance parameters are extracted from 2-port network S-parameter measurements, which are made using vector network analyzer R&S ZVRE. As three-phase filter is not a 2-port network, it is modified to enable correct 2-port network measurements, as shown in Fig. 4.3.b. However, insertion loss measurements are not in compliance with standard EN55017 [29], due to performed modifications, but it enables simple mutual coupling extraction and indicates main couplings that have impact on filter insertion loss. Mutual couplings are extracted using methodology that is stated in [15], [48].

Considering coupling polarities in Fig. 4.3a., equivalent circuit can be created in Fig. 4.4., that enables simple mutual coupling calculation from measured S-parameters, treating circuit as two port network. Coupling is called positive, if the capacitor branch equivalent inductance is positive and coupling is called negative if the capacitor branch equivalent inductance is negative [26].

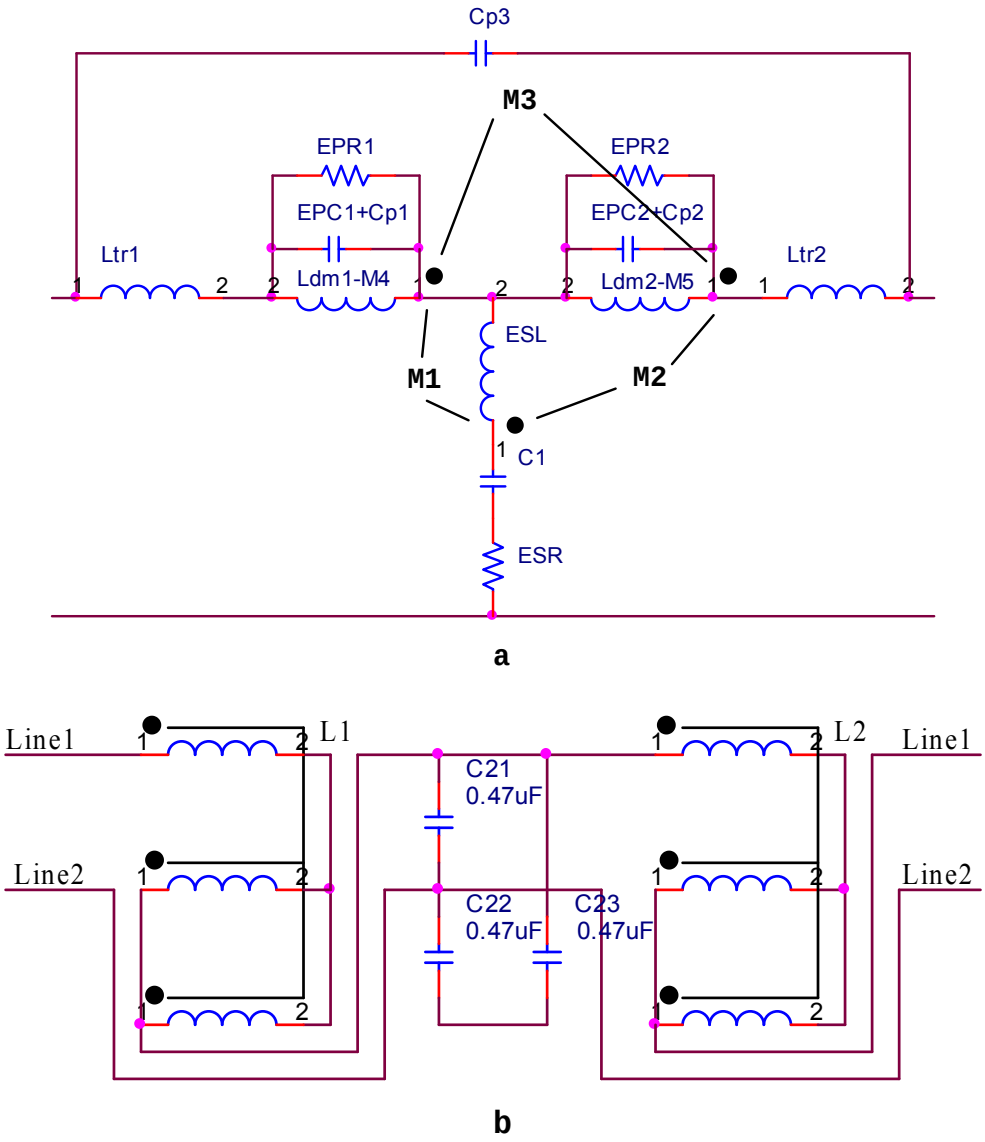


Fig. 4.3. a) Differential mode model of three phase filter, b) Three phase filter modification to enable 2-port S-parameter measurements

In the case if few couplings exist at the same time, the total effect determinates the coupling polarity. Capacitor branch impedance Z_C resonance frequency incorporating mutual inductance M can be calculated using expressions derived in section 2, for all type of couplings.

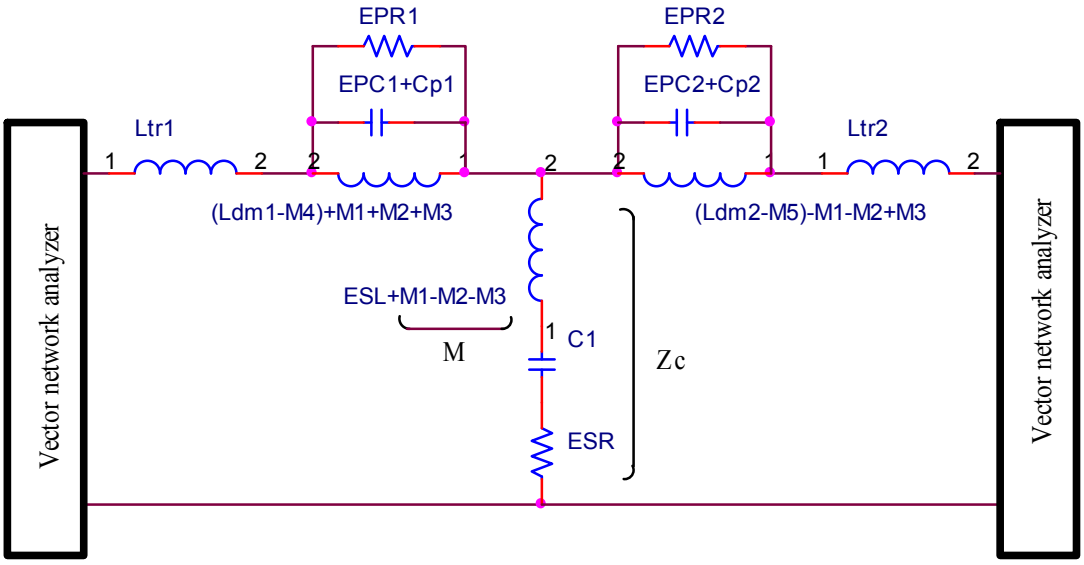


Fig. 4.4. Equivalent schematic of couplings with common mode chokes

Capacitor branch impedance Z_C is extracted from S-parameter measurements using (2-47) and using measurement setup in Fig. 4.3.b.

4.3 Mutual couplings created by common mode chokes

Capacitor branch C1 impedances and angles with and without couplings for filter with vertical CM chokes are plotted on Fig. 4.5. and with horizontal CM chokes plotted in Fig. 4.6. Using the measured data, mutual couplings M1, M2 and M3 are extracted and stated in Table 4.1.

The coupling polarity and magnitude strongly depends on the CM choke construction (distribution of leakage inductance flux, whose are responsible for DM inductance).

Table 4.1.

Mutual inductance of three phase filters with vertical and horizontal common modes

CM choke type	M1 (nH)	M2 (nH)	M3 (nH)	M4 (uH)	M5 (uH)
Horizontal	-22.4	3.46	-85	0.46	0.27
Vertical	12.6	-1.1	-80.4	0.49	0.48

There are no such possibilities of winding configurations for three phase CM chokes as for one phase common mode chokes as described in [41], so here are two types of CM chokes examined

- horizontal and vertical placement configurations. The cores of both chokes are made from the same ferrite material, the number of winding turns is the same and the winding placement on cores is equal.

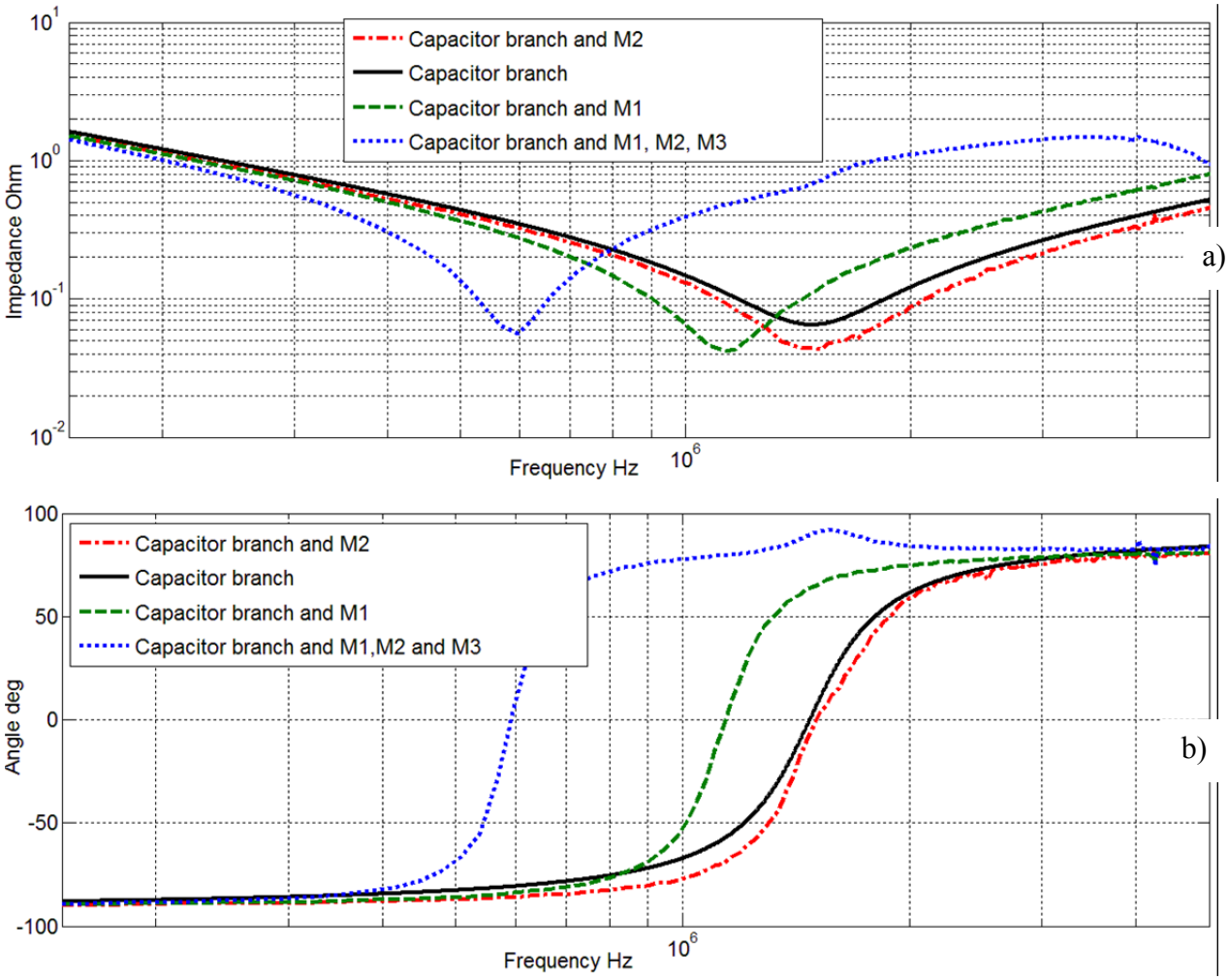


Fig. 4.5. Capacitor branch C1 impedance: a) magnitude with M1, M2 and M3 inductive couplings with vertical CM chokes, a) phase angle

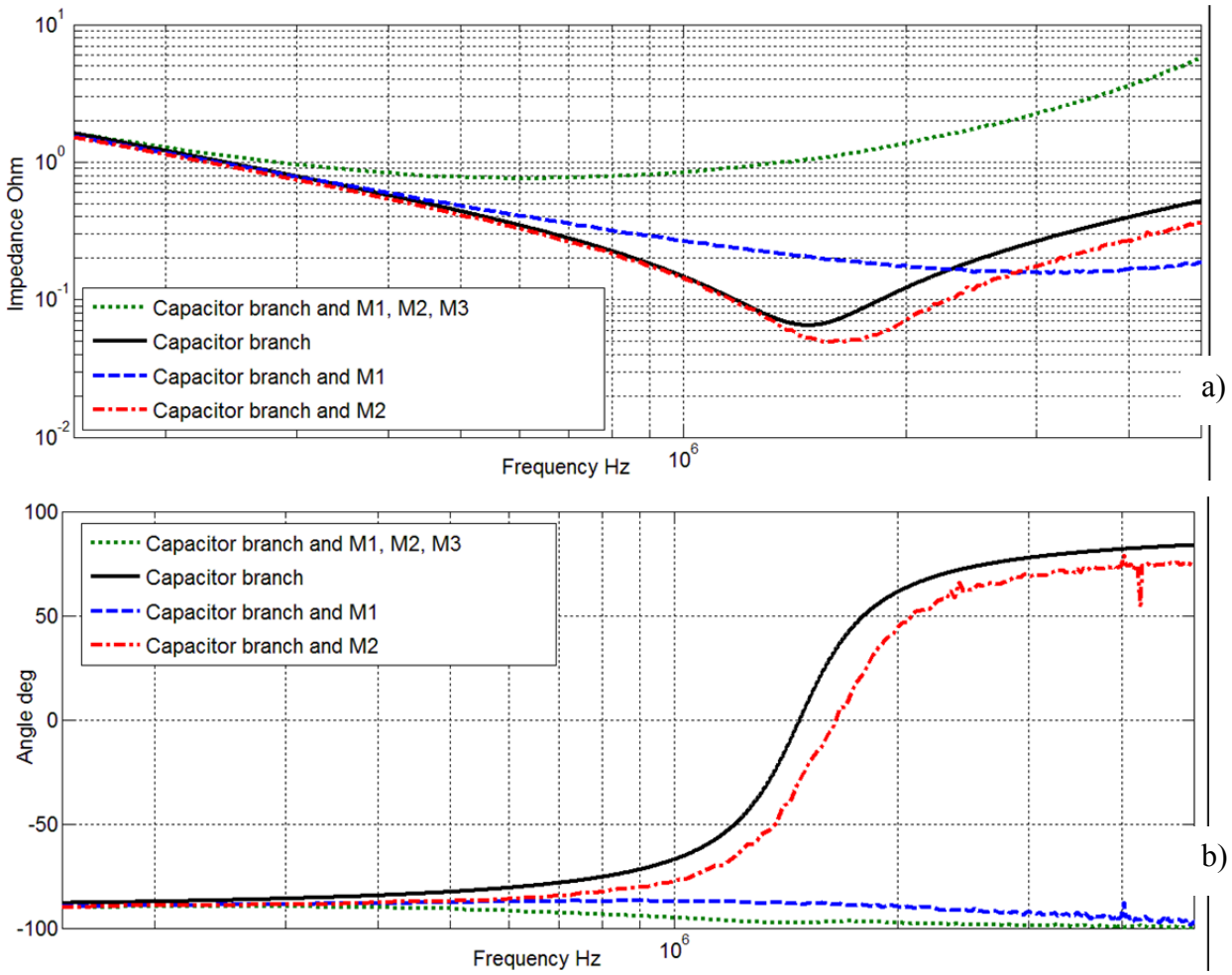


Fig. 4.6. Capacitor branch C1: a) impedance magnitude with M1, M2 and M3 inductive couplings with horizontal CM chokes, b) phase angle

4.4 Mutual couplings created by PCB

Mutual coupling C_{p1} and C_{p2} represents total coupling of parasitic capacitance in parallel with CM choke equivalent parasitic capacitance- EPC, when choke is mounted on PCB. For high frequency noise, coupling C_{p1}, C_{p2} and parasitic capacitance of CM choke creates a high frequency shortcut between input and output.

Coupling M4 and M5 is CM choke coupling to ground plane- the leakage flux created eddy currents in ground plane of PCB. This coupling is extracted using S-parameter measurements as in [15]. Impedances of CM chokes are calculated using the same manner as in previous chapter. Data on vertical and horizontal CM chokes are grouped in Table 4.2.

Mutual coupling C_{p3} is a coupling between input and output traces through ground plane of PCB. C_{p3} is measured directly using vector network analyzer when all components are dismounted from PCB.

Input and output trace inductances Ltr1 and Ltr2 are calculated in the same manner as CM choke inductances, when measurement probes are not directly connected to CM choke, but are connected through traces on PCB.

To show the importance of CM choke type and mutual couplings, measured filter one phase insertion loss (S_{21} or forward voltage gain) are compared in Fig. 4.7., further, as reference the same filters are modeled without couplings. As both models are almost identical, if mutual couplings are removed, in Fig. 4.7. only filter with vertical CM chokes is modeled, when the mutual couplings are absent.

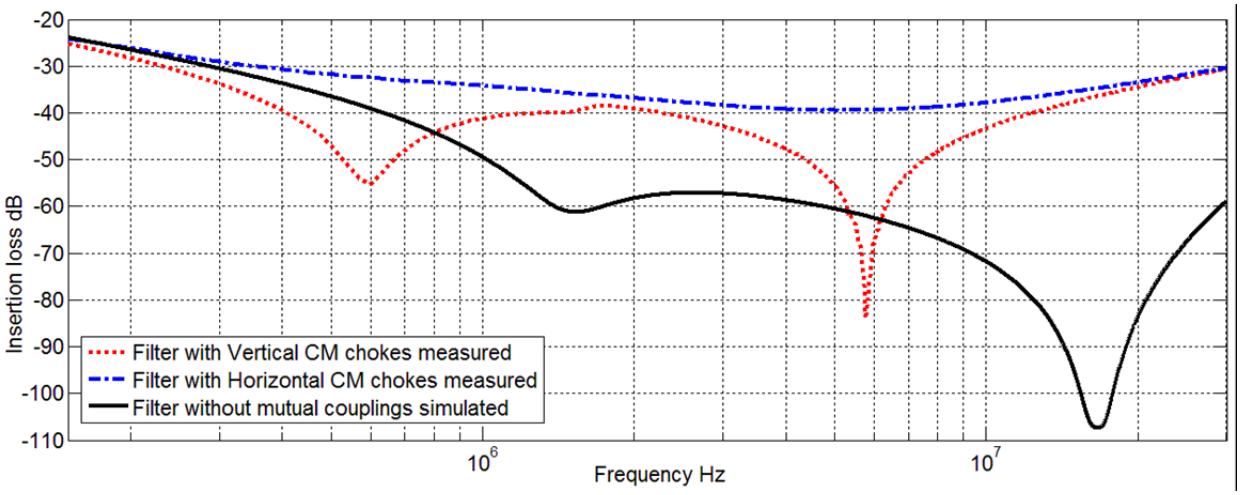


Fig. 4.7. Insertion loss of three phase filter one phase

Table 4.2.

Vertical and horizontal common mode chokes parasitic parameters

CM choke	L_{DM} (uH)	EPC (pF)	Cp (pF)	EPR (Ω)
Horizontal L1	6.98	7	6	9008
Horizontal L2	6.88	9	6	7856
Vertical L1	7.43	11	3	6573
Vertical L2	6.94	10	3	7760

4.5 Filter one phase differential mode model

Using extracted mutual couplings M1, M2, M3, M4, M5, C_{p1}, C_{p2}, and C_{p3} differential mode models of three phase filters one phase pair can be built and verified. Model is built and simulated in PSpace, using all extracted mutual inductances, capacitive couplings and self parasitics of filter components. Created models of filters with vertical and horizontal CM chokes, with component self parasitics and mutual inductances, parasitic capacitances are shown on Fig. 4.8. and Fig. 4.9.

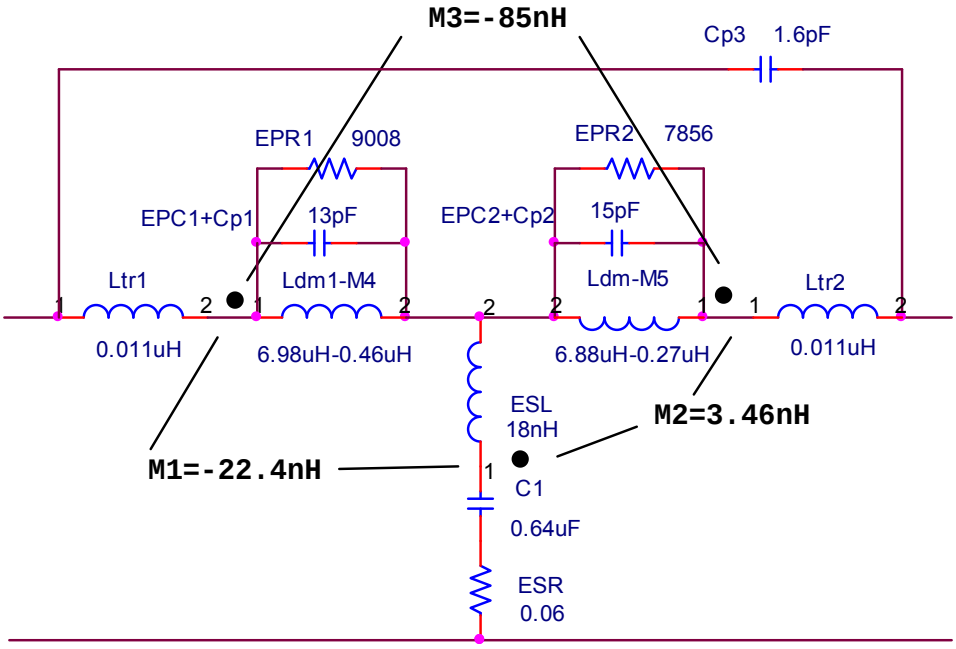


Fig. 4.8. Extracted DM model of three phase filter one phase with horizontal CM chokes

Real filters DM insertion loss and simulated insertion loss of both created filter models are displayed in Fig. 4.10 and Fig. 4.11. Insertion loss measurements of three phase filter are made using R&S vector network analyzer ZVRE, thus 50Ω measurement system is used. Also the modeling is done using 50Ω characteristic system impedance to compare measured and simulated data.

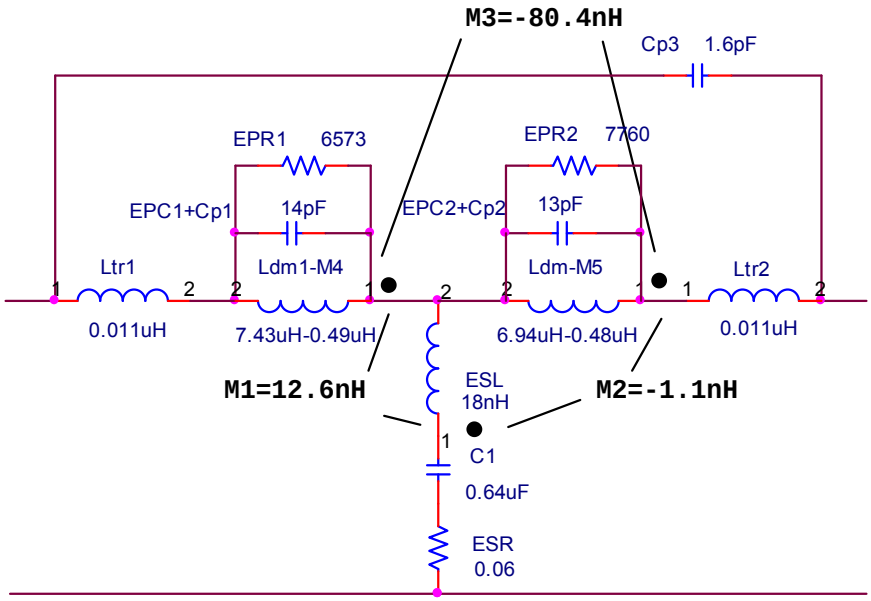


Fig. 4.9. Extracted DM model of three phase filter one phase with vertical CM chokes.

Simulated and measured insertion loss of both filters match very closely, so, the created models of three phase filter one of the phases are valid. Also the extraction procedures of mutual inductances and capacitive couplings are valid for three phase filters, equally as for one phase filters [41] and [15]. The created model can be used to explore all relevant parasitic parameters that are critical for filter performance and parasitic parameters that have negligible effect on filter performance, in such way most important parasitics are located and further approaches to cancel them can be carried out.

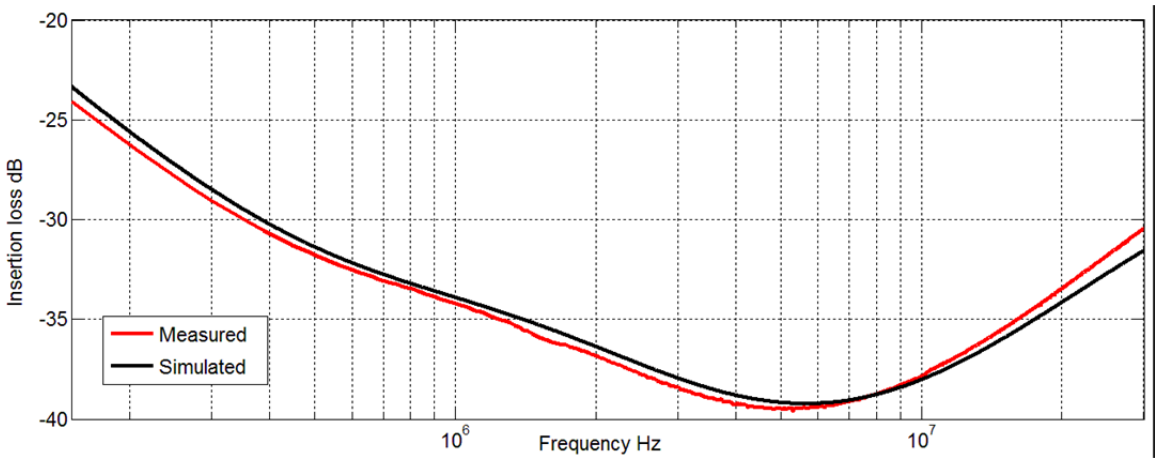


Fig. 4.10. Measured and simulated insertion loss of three phase filter one phase with horizontal CM chokes

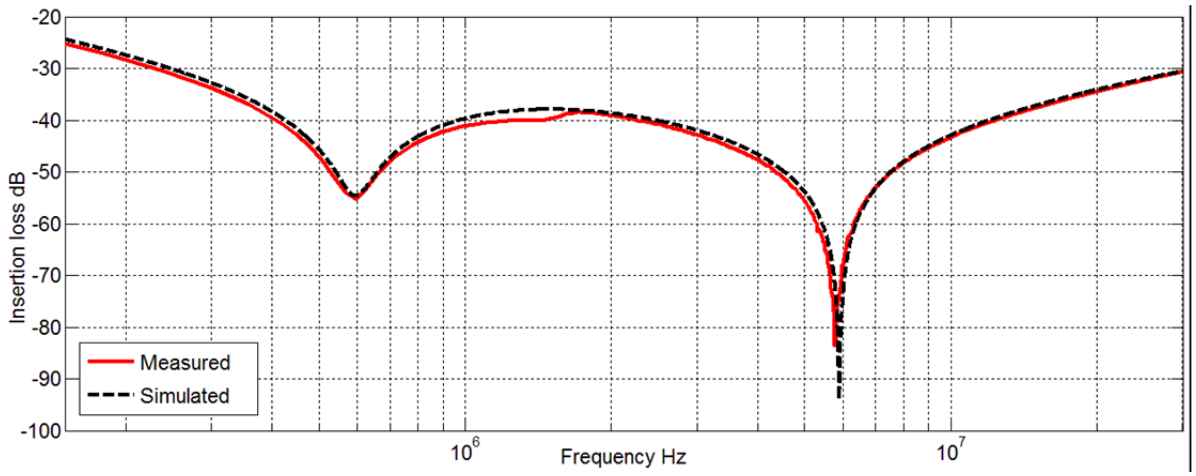


Fig. 4.11. Measured and simulated insertion loss of three phase filter one phase with vertical CM chokes

4.6 Mutual coupling influence analysis on three phase T-type filter insertion loss

Based on created models in

Fig. 4.8. and Fig. 4.9. the most important mutual couplings are discovered that are mainly responsible for insertion loss reduction. The most important mutual coupling, in frequency range up to few MHz, appears M3 that couples both CM inductors. The situation is shown in Fig. 4.12. for filter with horizontal CM chokes and Fig. 4.13. for filter with vertical CM chokes. In case if only M3 mutual coupling is eliminated both types of filters provide almost identical insertion loss.

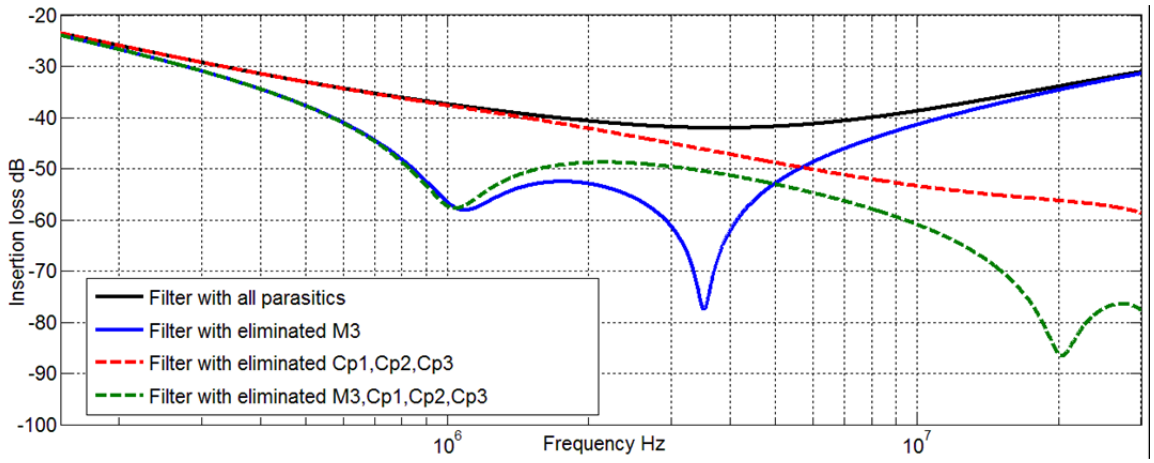


Fig. 4.12. Simulated insertion loss of three phase filter one phase, with horizontal CM chokes, with eliminated parasitics

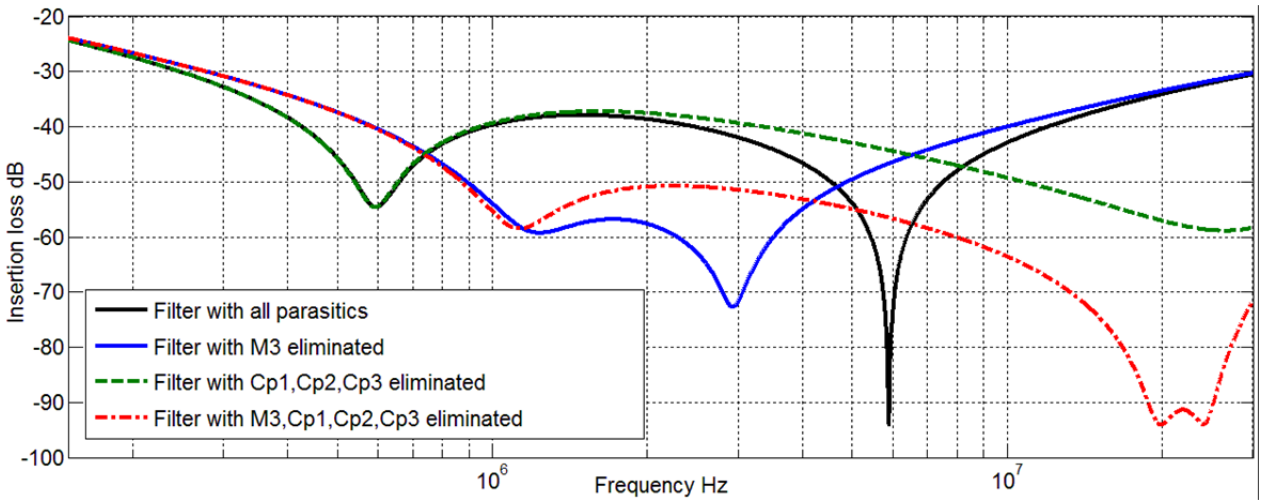


Fig. 4.13. Simulated insertion loss of three phase filter one phase, with vertical CM chokes, with eliminated parasitics

As in both filter types magnitude of M3 is almost equal, the coupling polarity between L1 and L2 in relation to other coupling polarities in the filter is the most important key factor. Coupling M3 between L1 and L2 provides shortcut for high frequency disturbances, therefore the coupling magnitude and polarity in relation to other couplings can decrease or increase coupling effect on high frequency insertion loss as it can be seen in Fig. 4.10 and Fig. 4.11.

In frequency range above few MHz capacitive couplings Cp1, Cp2, Cp3 are critical parasitics. Actually, capacitive couplings couples directly high frequency disturbances from filters input to output and other components have little impact on this process, as it can be seen in Fig. 4.12 and Fig. 4.13. Therefore mutual coupling M3 and capacitive coupling Cp elimination on both types of filters are key factors to improve filters performance especially in high frequency region.

4.7 Conclusions

Mutual couplings between three phase components- capacitors and CM chokes have an impact on filter insertion loss, as well as couplings created by PCB traces and ground plane, as it can be seen in Fig. 4.7, where ideal filter without mutual couplings is modeled as a reference to measured real filters.

Common mode choke alignment (vertical or horizontal) has an influence on mutual couplings M1, M2, M3, but it can't be concluded that vertical or horizontal CM chokes are more suitable for higher or lower frequencies as in previous chapter. Also, coupling polarities on capacitor branch C1 are not directly connected to CM choke placement- horizontal or vertical. Coupling polarities depend on CM choke winding placement in respect to capacitors, created resultant from leakage inductance.

CM choke differential mode inductance- leakage inductance is affected by near PCB ground plane decreasing it. In fact, results in Table 4.2. show that CM choke alignment over PCB ground plane have similar effect on both CM choke types.

Although, three phase filter modification in Fig. 4.3.b to enable two port network measurements, with vector network analyzer to calculate insertion loss, is not compliant with EN55017 standard, therefore measurement method enables simple extraction of mutual couplings and gives opportunity to evaluate their impact magnitude on insertion loss. Experiments with two type CM chokes have shown that component to component mutual coupling magnitudes are quite similar-

Fig. 4.8, Fig. 4.9. However, coupling polarities affect insertion loss characteristic seriously as it can be seen in Fig. 4.7. The most important coupling is M3 that couples two CM inductors. In case if coupling M3 between L1 and L2 is negative, insertion loss of filter increases, otherwise high frequency shortcut is created between input and output. Parasitic capacitances C_{p1}- C_{p3} also are very critical parasitics, especially in high frequency region that creates high frequency shortcut between input and output.

5. CAPACITORS MUTUAL INDUCTANCE MODELING

5.1 Background

In EMI filter, components are mounted next to each other as close as possible, leading to mutual couplings [17] degrading filter performance. Various measurement techniques for mutual coupling measurement [49], [17], extraction [50], mutual coupling reduction [51] and optimization [18], [19], [20] have been presented. Therefore, there is still lack of information on techniques and possibilities, using in market available, the most popular 3D electromagnetic modeling tools that could help to solve these problems in more effective manner. However, there are some articles that have described 3D electromagnetic modeling tools in EMI filter modeling [21], [22], [23], but these are not the industry driven 3D electromagnetic modeling tools. In this chapter there is EMI filter capacitor modeling and capacitor mutual coupling modeling proposed. Three capacitor models are proposed and verified [52].

5.2 Prototype PCB modeling and verification

Two prototypes PCB's have been created for mutual inductance measurements. Both boards have the same dimensions, material properties and connectors. The difference is only in width of copper tracks. For prototype PCB1, the track width is made maximal- leaving only 1mm clearance between the tracks, Fig. 5.1. For prototype PCB2 the track width is made minimal- leaving it to 5mm in width and track clearance 17.5mm, Fig. 5.2. In prototype PCB1 the recommendations [53] have been taken into account, to lower the capacitor ESL and ESR. Therefore PCB2 have been created to violate these rules and analyze the impact on mutual inductance between the capacitors. Also 3D models of both prototypes have been created, see (Fig. 5.3. and Fig. 5.4.). Models of both prototypes are created in CST MWS [54]. Board insulation material is FR4 (loss free). All conductive parts of models are modeled as PEC- perfect electrical conductors. The insulator for SMA type connector is Teflon (PTFE) (loss free). All 3D model materials are chosen from default material library without any parametric modifications.

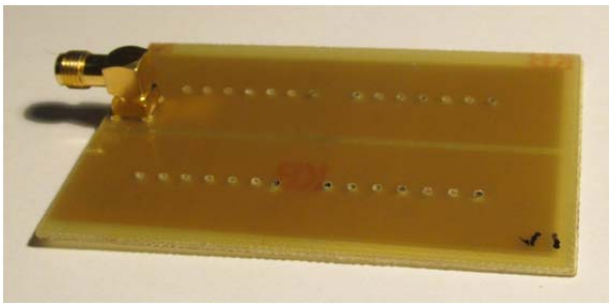


Fig. 5.1. Prototype PCB1 used for mutual inductance extraction between capacitors

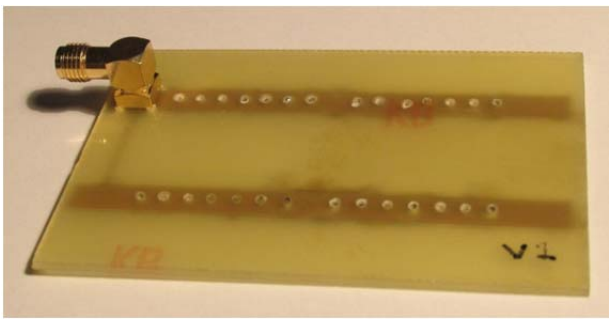


Fig. 5.2. Prototype PCB2 used for mutual inductance extraction between capacitors

To reliably start to model capacitors on PCB, 3D models of prototype PCB1 and PCB2 have to be validated. Validation is done by short circuiting both prototypes and measuring the impedance at SMA port.

Measurement and modeling results are presented on Fig. 5.5. Measurement results below 100kHz are noisy due to the fact that low impedance is measured and measurement method that uses VNA does not have the highest accuracy when very low impedances are measured. It can be concluded that 3D models of both prototypes are well built as modeling and measurement results fit quite well. The measured impedance has inductive characteristic. It is obvious, as the short circuited PCB's create loops. Prototype PCB1 impedance is lower than PCB2 impedance, due to the fact that it has tracks with a higher cross section area and tracks are creating loop with a smaller area. Higher track cross section area and smaller loop area should lead also to lower impedance when capacitors will be mounted on PCB's.

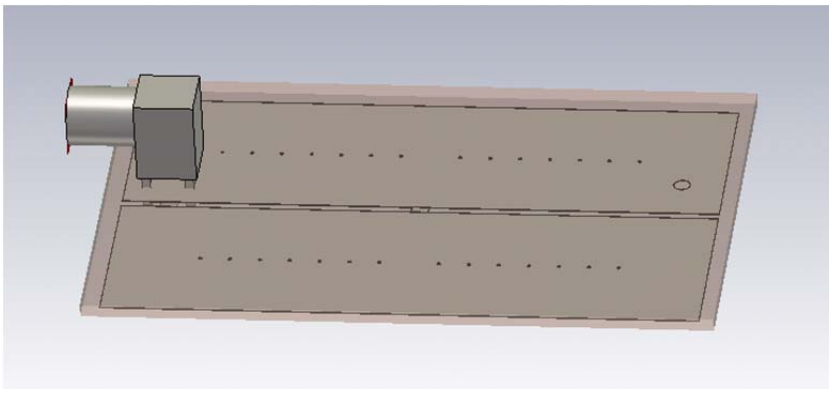


Fig. 5.3. 3D model of prototype PCB1 that is used for validation

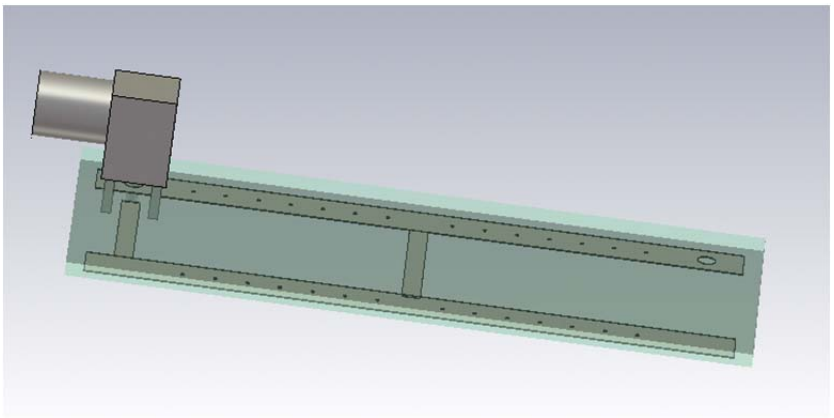


Fig. 5.4. 3D model of prototype PCB2 that is used for validation

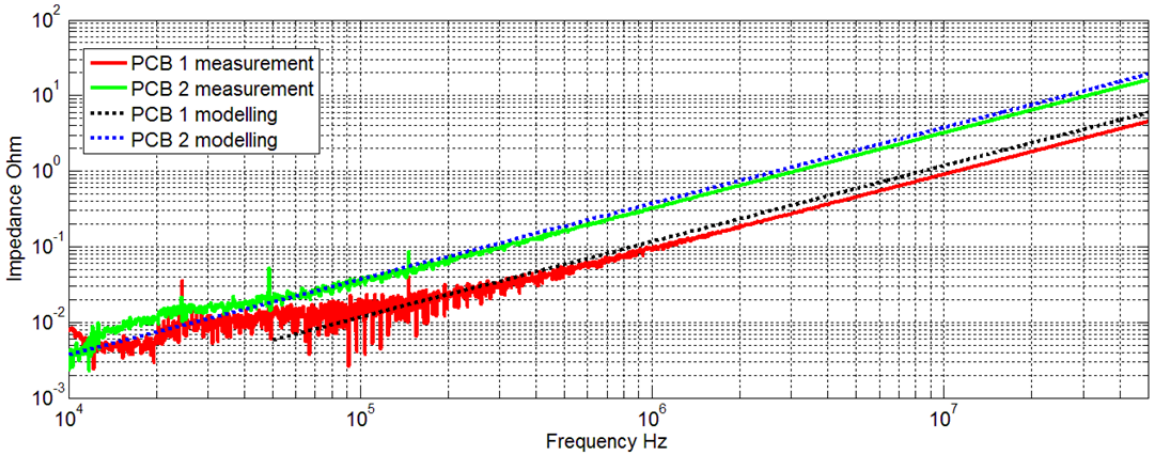


Fig. 5.5. Two PCB Prototype verification results

5.3 Capacitor modeling

Capacitor is made of several thousands of metalized film layers Fig. 5.6. Obviously, it is not appropriate to describe the exact internal geometry with all the layers, as it takes huge

amount of memory and huge amount of computational power, to solve the task. Therefore, homogenization technique in literature, associated to simplified geometry [19] is proposed. Like Dowell method [55] the resistivity is adapted. Electrode count is adapted to trade of current division among several paths and limit increase of the geometrical complexity, Fig. 5.7. The extremities of connectors are connected using perfect electrical conductors. This kind of models represent capacitors magnetic behavior only, and have to be improved with a series capacitance. Magnetic behavior of component model provides ESR and ESL, including couplings with the environment.

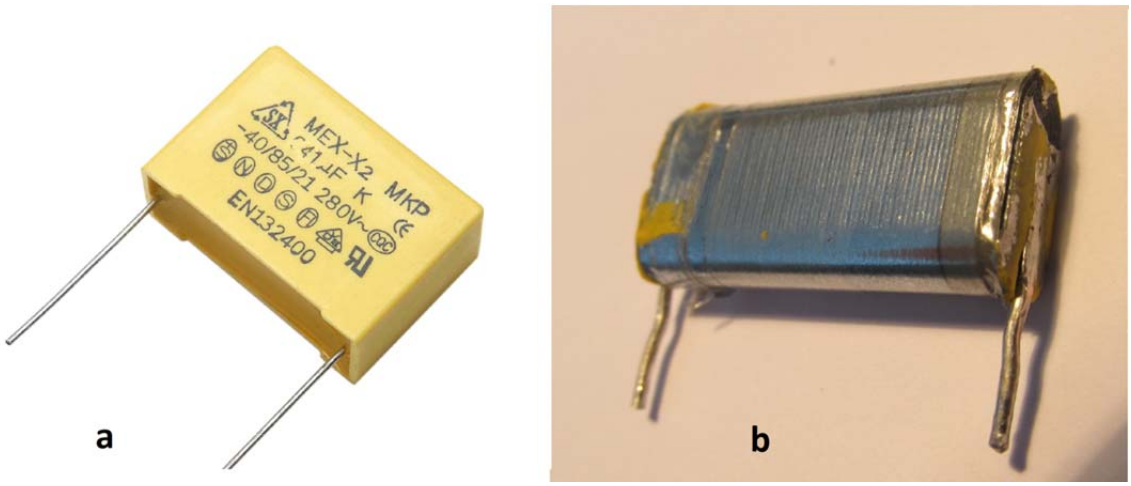


Fig. 5.6. Capacitor used for measurements: a) intact capacitor, b) inner structure of capacitor

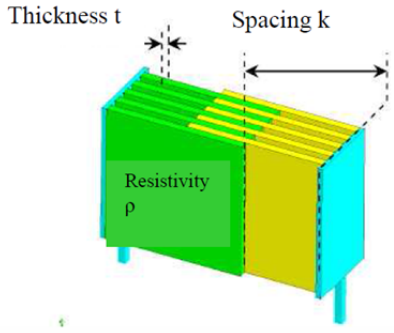


Fig. 5.7. Capacitor model proposed in literature

This model is still complex from point of view of modeling- lot of surfaces and details to mesh. Therefore, [19] proposes further simplification in Fig. 5.8., regarding the actual component geometry, where only one electrode is present. The current is supposed to circulate along single electrode and thus the modeling is less power and memory consuming. This model also describes magnetic behavior and provides ESR and ESL, including couplings with the environment.

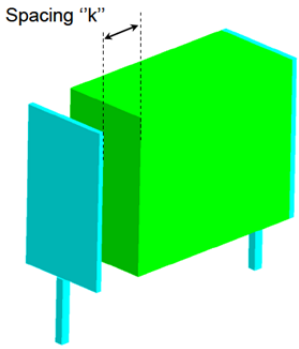


Fig. 5.8. Simplified capacitor model for 3D electromagnetic modeling

Both models proposed in [19] must be calibrated and the variables of resistive part of component calculated- electrode spacing- k, thickness- t, resistivity- ρ while the rest of the geometry is fixed by the actual component size.

It is possible to propose much simpler model that eliminates the usage of conductive material and is more suitable for usage with modern 3D electromagnetic modeling software as ANSYS HFFS and CST MWS. In this case the capacitor capacitance C and ESR must be represented by lumped elements. The structure of model is made out of perfect electric conductor. The physical size of models represents exact size of capacitor conductive parts, without outer insulation shell, as in Fig. 5.6.b. Three models are proposed, starting from most complex, that represents the inner structure of capacitor more detailed- Cap1, to the less complex- Cap3, that leads to the lowest memory consumption and computational power Fig. 5.9.

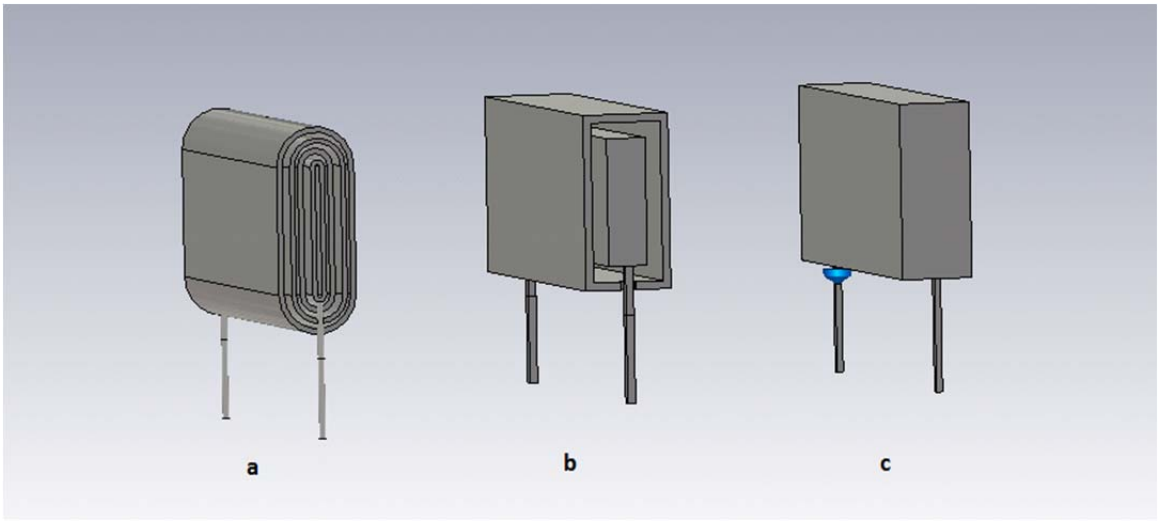


Fig. 5.9. Capacitor models: a) the most complex capacitor model proposed- Cap1; b) medium complex capacitor model proposed- Cap2; c) the simplest capacitor model proposed- Cap3

The first two proposed models- Cap1 and Cap2, in plain manner represent the capacitor metalized film layer structure, to verify the coupling properties to nearby components. The Cap3 model is modeled as rectangle and does not represent inner metalized film layer structure, but only the exact overall dimensions of capacitor conductors. Capacitor models also represent only magnetic behavior of component, thus they are supplemented by capacitance and series resistance using lumped elements. In CST MSW the capacitors can be meshed using tetrahedral and hexahedral mesh. The meshcell number is compared for all capacitor prototypes in Table 5.1. All the boundary settings, materials and mesh settings are the same for all models. It should be mentioned that no optimization of mesh setting have not been done to evaluate the situation for all models in the same conditions.

Table 5.1.

Meshcell count for proposed capacitor models

	Capacitor model		
Mesh type	Cap1 Meshcells	Cap2 Meshcells	Cap3 Meshcells
Tetrahedral	85.474	25.219	16.878
Hexahedral	47.376	22.644	18.432

The least complex capacitor model- Cap3, has the least complex mesh that leads to the lowest meschell number.

Mesh and calculation time can be compared to evaluate all three capacitor models. CST MSW provides wide amount of solvers to use. Time domain and frequency domain solvers have been chosen, to use, for problem solving. Frequency domain solver can be used with tetrahedral and hexahedral mesh, while time domain solver only with hexahedral mesh type. In Table 5.2., modeling time for three capacitor models is compared for both solvers with different mesh types. For frequency domain only one frequency sample is calculated, while time domain solver calculates all the defined frequency range 100kHz-50MHz, therefore it should be mentioned that in Table 5.2. capacitor model calculation times are compared, not the solvers itself.

Table 5.2.

Meshcell number for proposed capacitor models

	Capacitor model

Solver/ mesh type	Cap1 h:min	Cap2 h:min	Cap3 h:min
Time domain/ Hexahedral	14:05	1:11	1:01
Frequency domain/ Hexahedral	1:10	0:26	0:20
Frequency domain/ Tetrahedral	2:40	0:51	0:32

Using both solvers and different mesh types it is obvious that Cap3 model calculation takes at least 30% less than Cap2 calculation and at least 250% less time than Cap1 calculation, if frequency domain solver with hexahedral mesh is used. For time domain solver the difference in calculation time is higher- Cap3 model calculation takes at least 16% less than Cap2 calculation and at least 1280% less time than Cap1model calculation.

In further sub-clauses the evaluation of all three models performance is verified and analyzed to prove that it is possible to model capacitors, used in EMI filters, using 3D electromagnetic modeling software with high accuracy, without describing capacitor with several thousands of metalized film layers.

5.4 Capacitor model verification

The capacitor models for further successful usage were validated. The set of S-parameter and Z-parameter measurements were carried out:

1) One capacitor mounted on PCB (Z_{11} measured),
2) Two capacitors mounted on PCB (Z_{11} measured),
3) Two capacitors mounted on PCB (S- parameters measured),
4) Two capacitors mounted on modified PCB, with one solid and one split track (S-parameters measured).

5.4.1 Z_{11} parameter measurements if one capacitor is mounted on PCB

To verify the performance of both- PCB and all proposed capacitor models, measurements were carried out and input impedance at SMA port were measured. The 3D models for PCB1 with mounted capacitors, with tetrahedral mesh view and measured prototype are shown in Fig. 5.10.

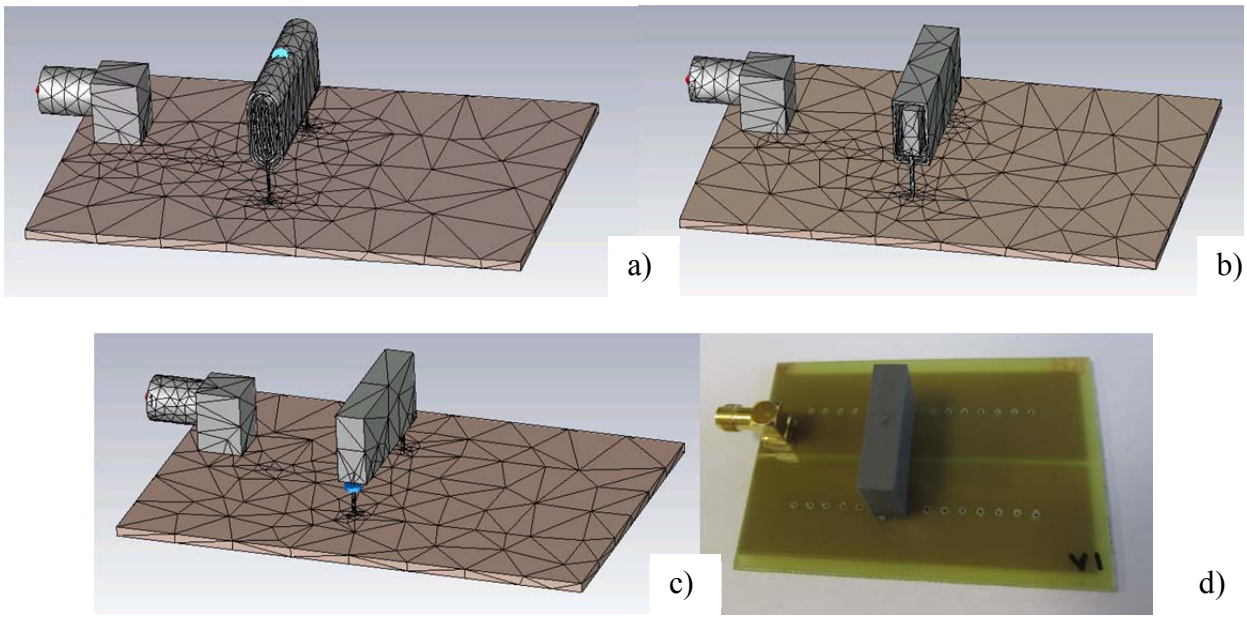


Fig. 5.10. 3D model of PCB1 with tetrahedral mesh and measured prototype: a) Cap1 model, b) Cap2 model, c) Cap3 model, d) measured prototype

The measurement and modeling results are compared in Fig. 5.11. and Fig. 5.12. for both PCB1 and PCB2, respectively. In this case impedance Z_{11} characterizes capacitor impedance, PCB layout impedance and interaction between capacitor and PCB.

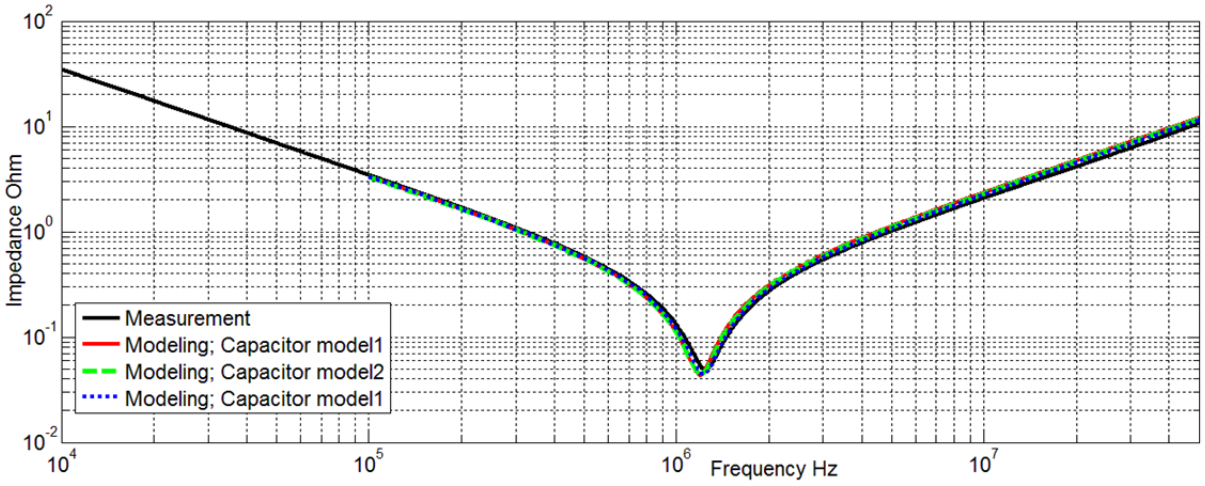


Fig. 5.11. Impedance magnitude of PCB1 and capacitor

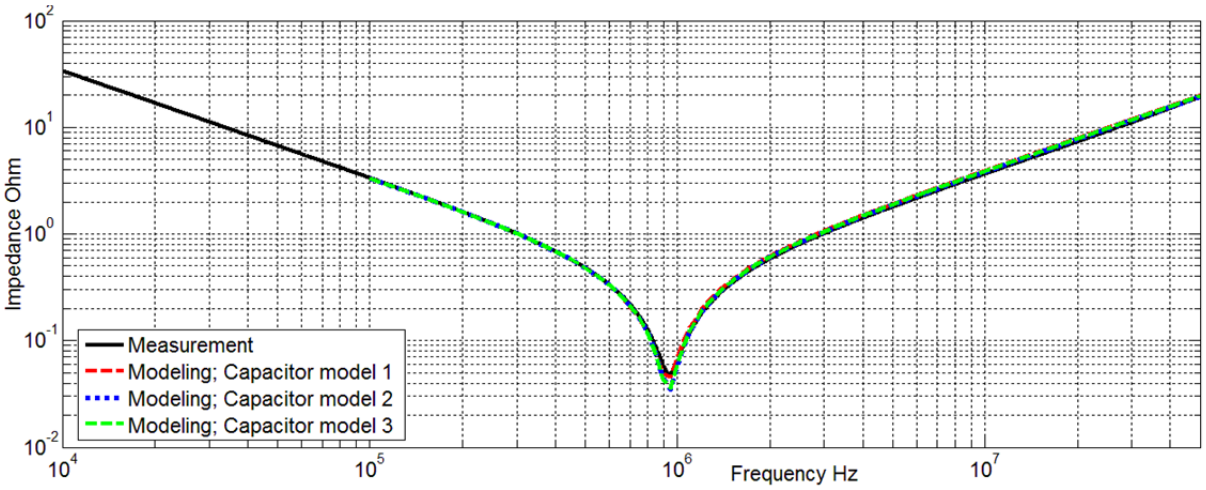


Fig. 5.12. Impedance magnitude of PCB2 and capacitor

Measurement and modeling results fit very well for all three proposed capacitor models. All three capacitor models provide almost identical impedance, therefore it can be concluded that their performance is equal in this current case.

5.4.2 Z_{11} parameter measurements if two capacitors are mounted on PCB

To verify the performance of both- PCB and all proposed capacitor models, measurements were carried out and input impedance at SMA port was measured. The 3D models for PCB1 with mounted capacitors, with tetrahedral mesh view and measured prototype are shown in Fig. 5.13. In this case two capacitors are mounted in different distances from each other: 7mm, 17.5mm and 28mm, respectively. Distance between capacitors is measured between capacitor central axis. Therefore, impedance Z_{11} characterizes capacitors impedance, PCB layout impedance, interaction between capacitors and PCB and interaction between two capacitors- that is mutual inductance between capacitors, mainly. The results were compared in Fig. 5.14. – Fig. 5.16. for PCB1 and in Fig. 5.17. – Fig. 5.19 for PCB2, when capacitors are mounted in different distances.

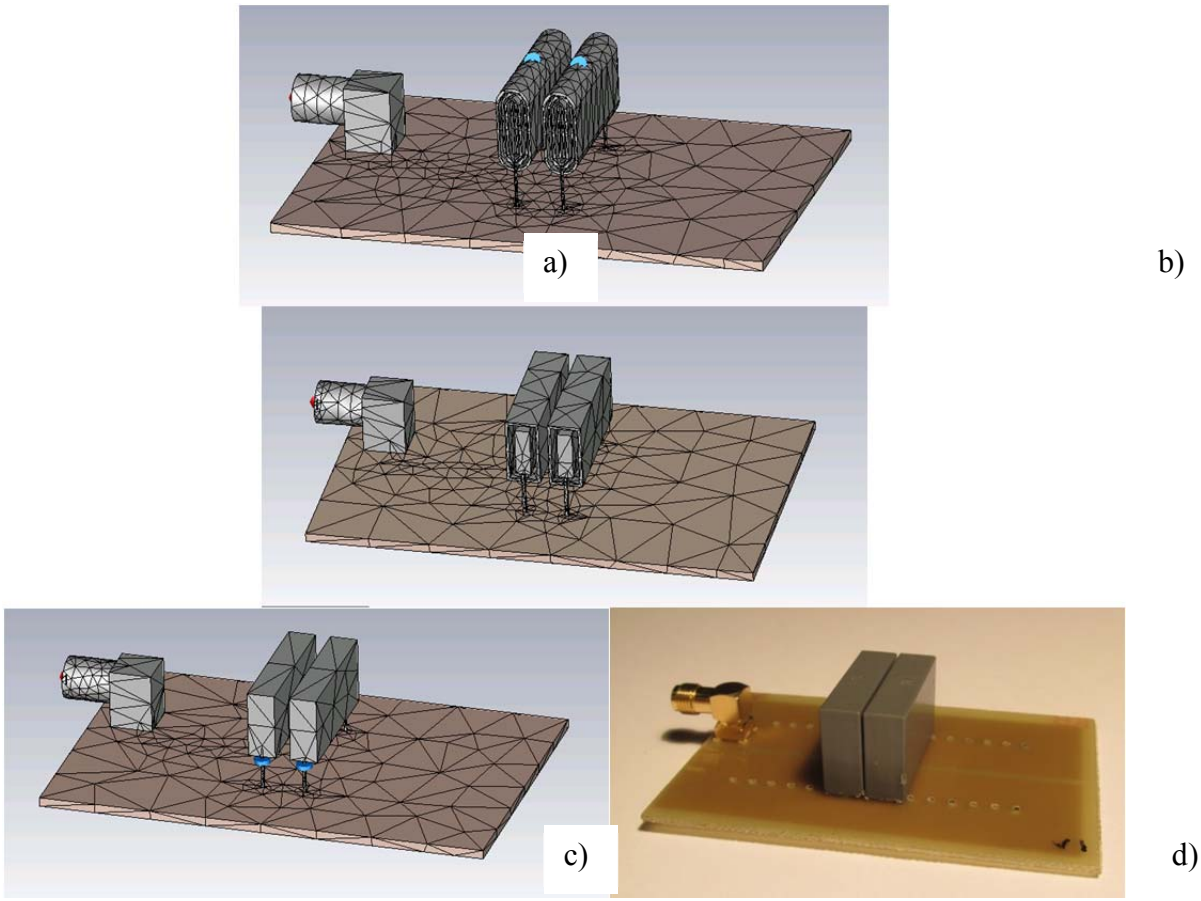


Fig. 5.13. 3D model of PCB1 with tetrahedral mesh and measured prototype, when capacitors are mounted in 7mm distance: a) Cap1 model, b) Cap2 model c) Cap3 model, d) measured prototype

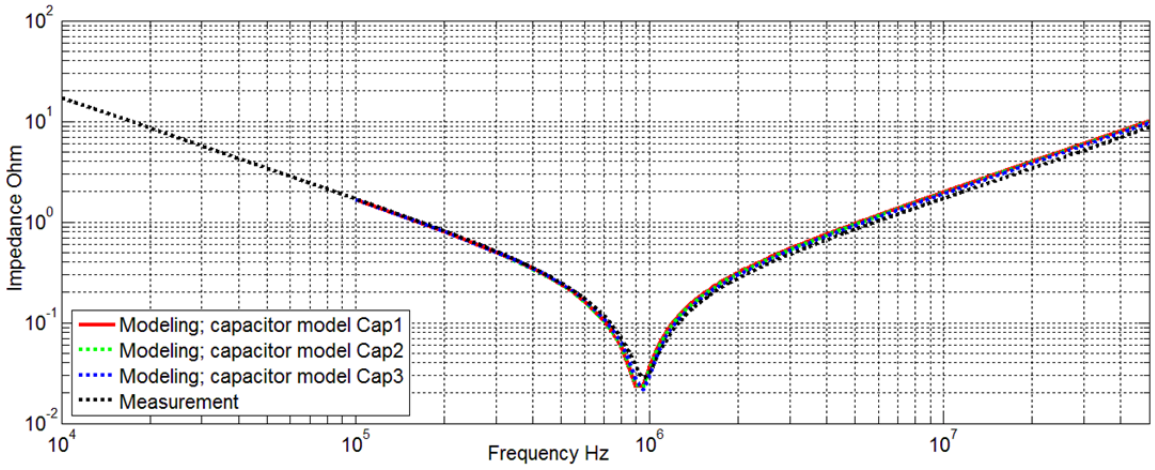


Fig. 5.14. Impedance magnitude of PCB1 and capacitors in 7mm distance

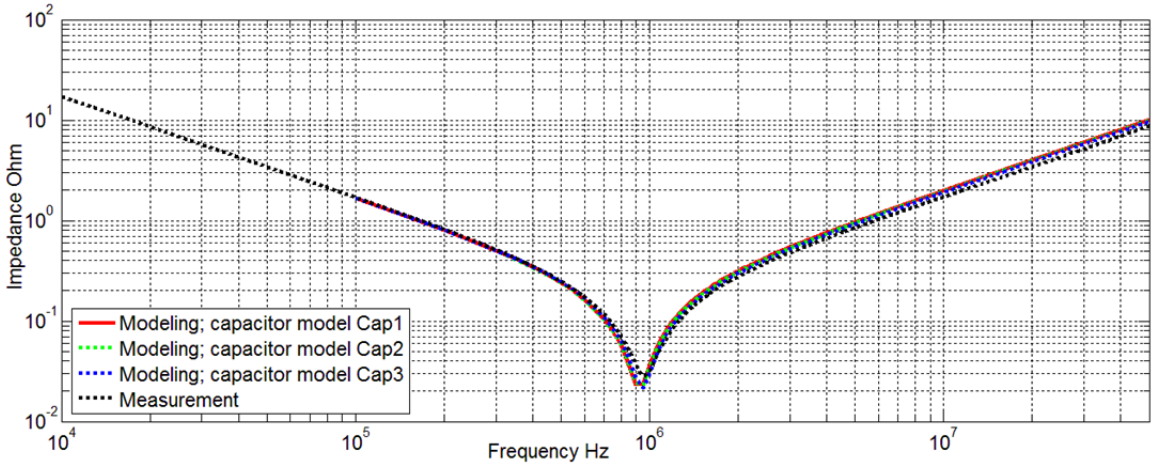


Fig. 5.15. Impedance magnitude of PCB1 and capacitors in 17.5mm distance

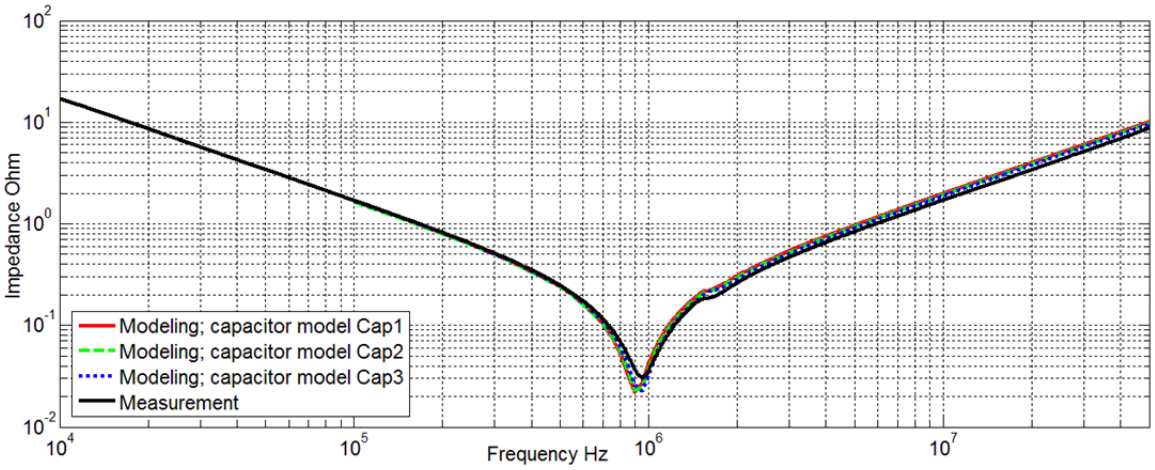


Fig. 5.16. Impedance magnitude of PCB1 and capacitors in 28mm distance

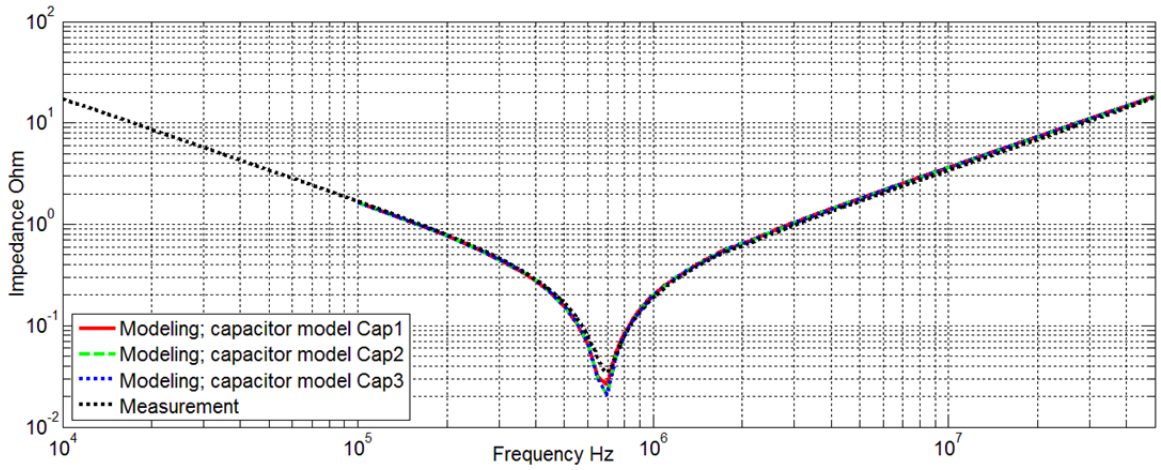


Fig. 5.17. Impedance magnitude of PCB2 and capacitors in 7mm distance

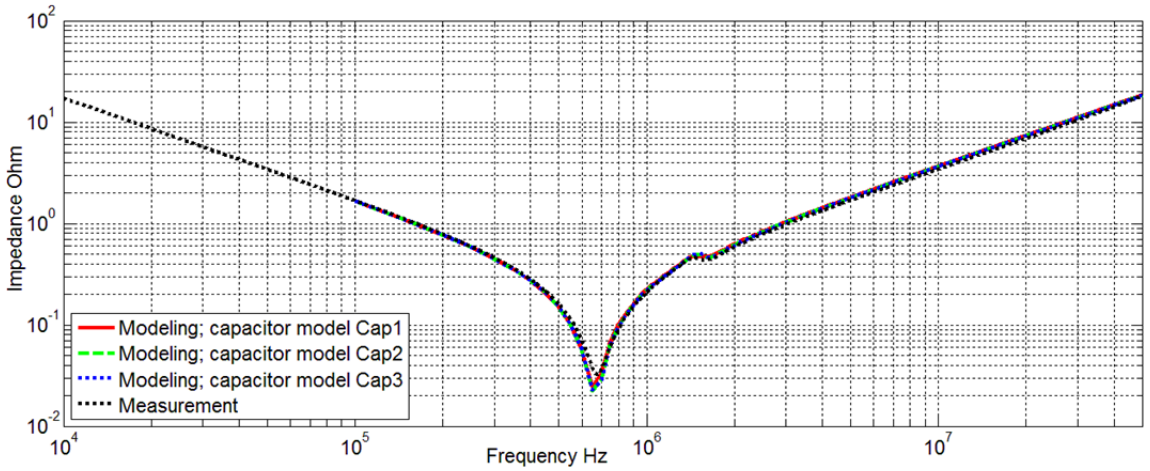


Fig. 5.18. Impedance magnitude of PCB2 and capacitors in 17.5mm distance

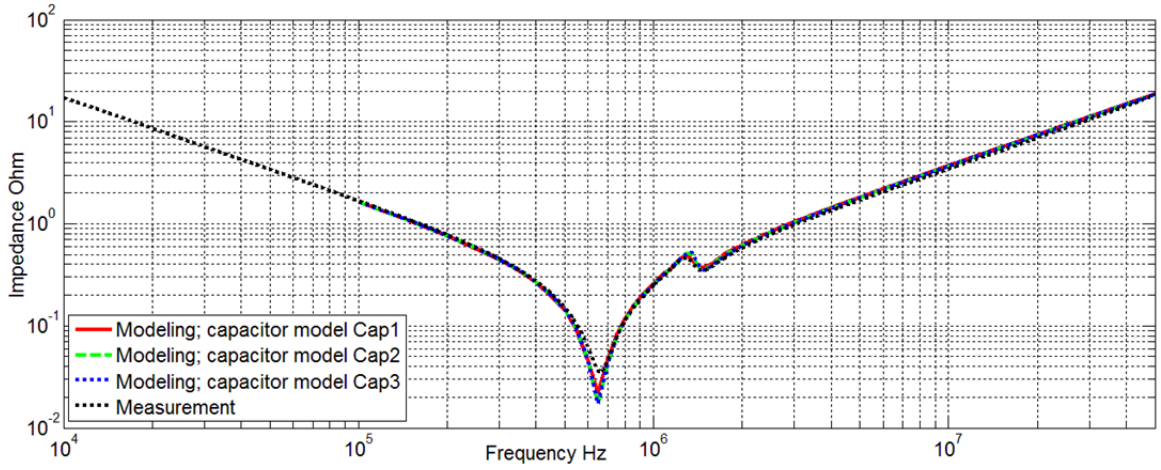


Fig. 5.19. Impedance magnitude of PCB2 and capacitors in 28mm distance

Measurement and modeling results match very well for all PCB and capacitor models. The modeling precision can be evaluated in Fig. 5.19., where resonance effect at 1.3MHz is modeled with high accuracy.

5.4.3 Two port S-parameter measurement if two capacitors are mounted on PCB

To verify the performance of both- PCB and all proposed capacitor models, measurements were carried out and two port S-parameters at SMA ports were measured. PCB's in this case are slightly modified. One of the copper tracks has a 2mm split in the middle. Therefore, S21 and S12 parameters characterize the coupling of two loops, created by PCB and capacitors- mainly mutual coupling. The 3D model for PCB1 with mounted capacitor and measured prototype are shown in Fig. 5.20.

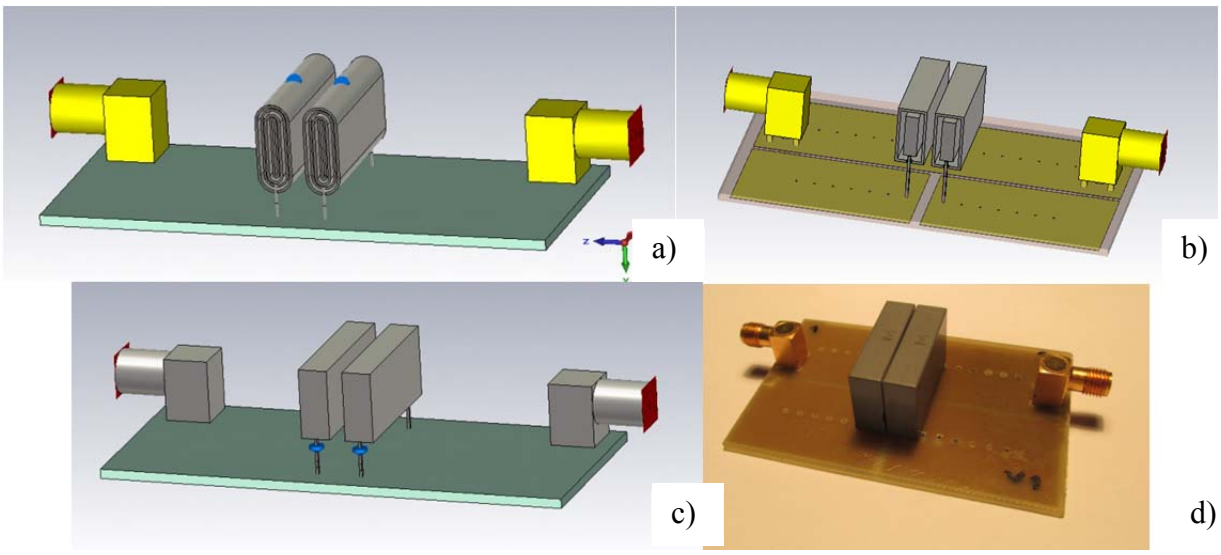


Fig. 5.20. 3D model of PCB1 with a split track and measured prototype when capacitors are mounted in 7mm distance: a) Cap1 model, b) Cap2 model (transparency of PCB insulator changed to see the split track), c) Cap3 model, d) measured prototype

Measurement and modeling results are compared in Fig. 5.21. – Fig. 5.26. It can be concluded that capacitor models- Cap1, Cap2, Cap3 give similar results and they are very close to modeling results for both PSB's.

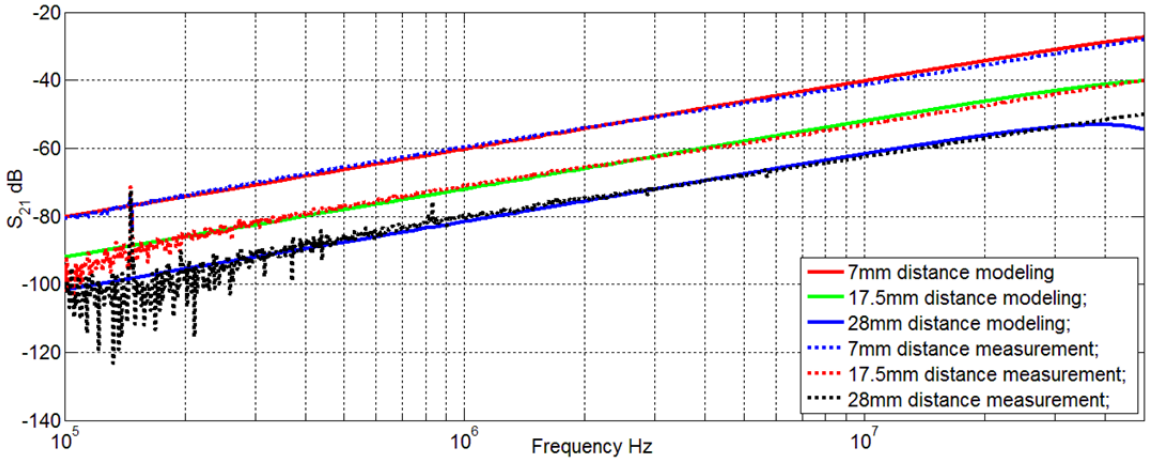


Fig. 5.21. Transfer characteristic of PCB1 with split track and capacitor model Cap1

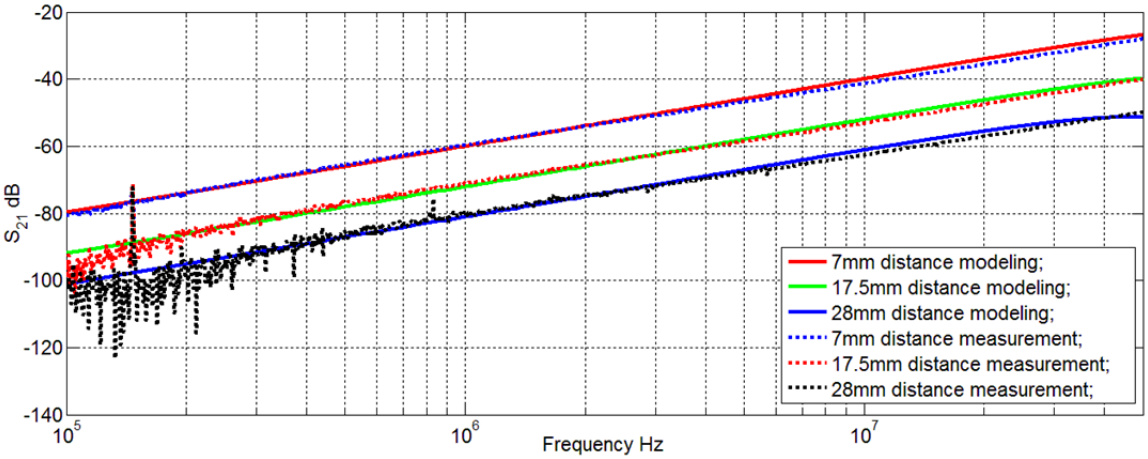


Fig. 5.22. Transfer characteristic of PCB1 with split track and capacitor model Cap2

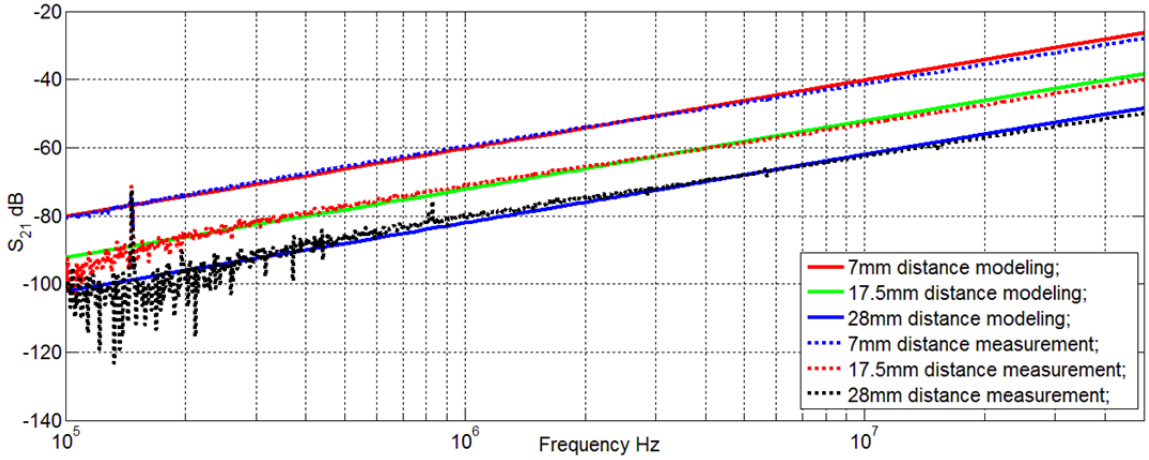


Fig. 5.23. Transfer characteristic of PCB1 with split track and capacitor model Cap3

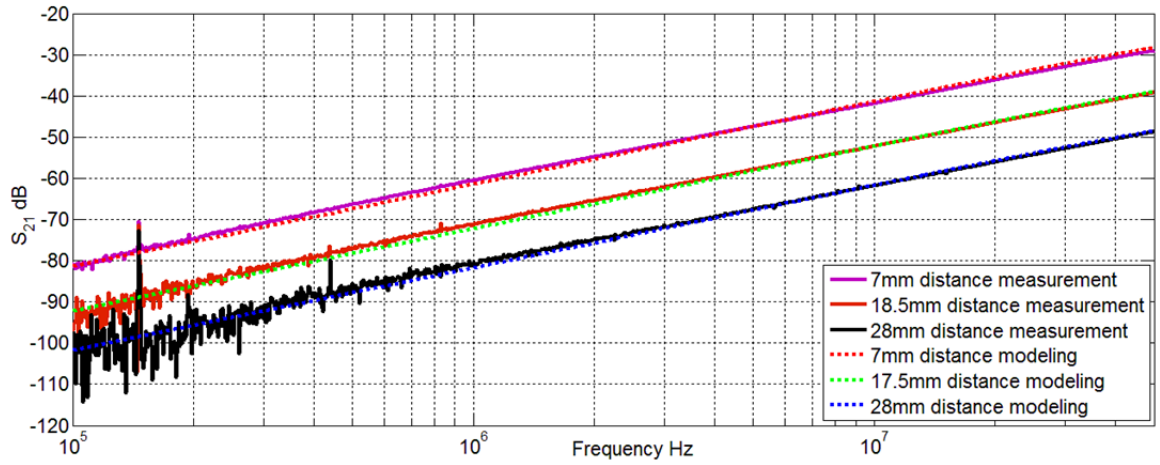


Fig. 5.24. Transfer characteristic of PCB2 with split track and capacitor model Cap1

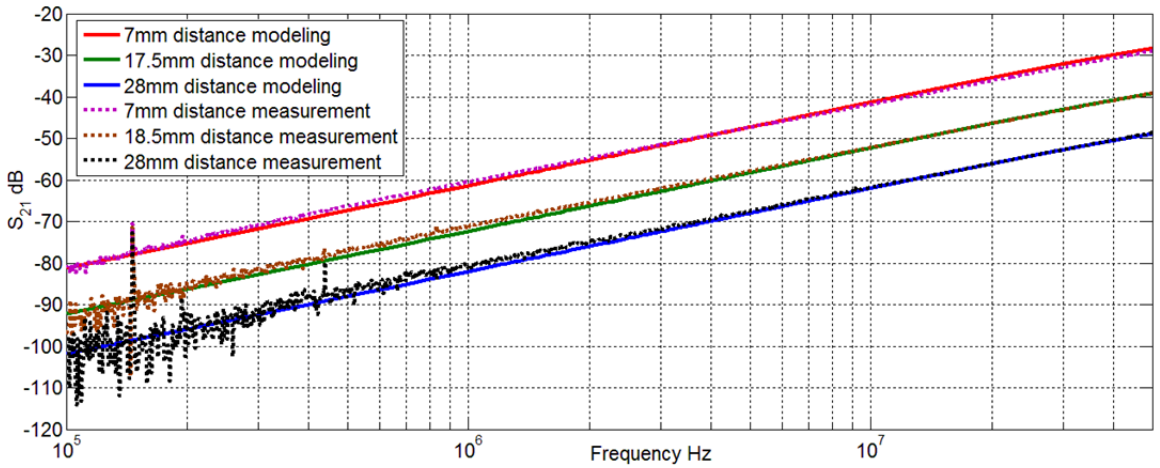


Fig. 5.25. Transfer characteristic of PCB2 with split track and capacitor model Cap2

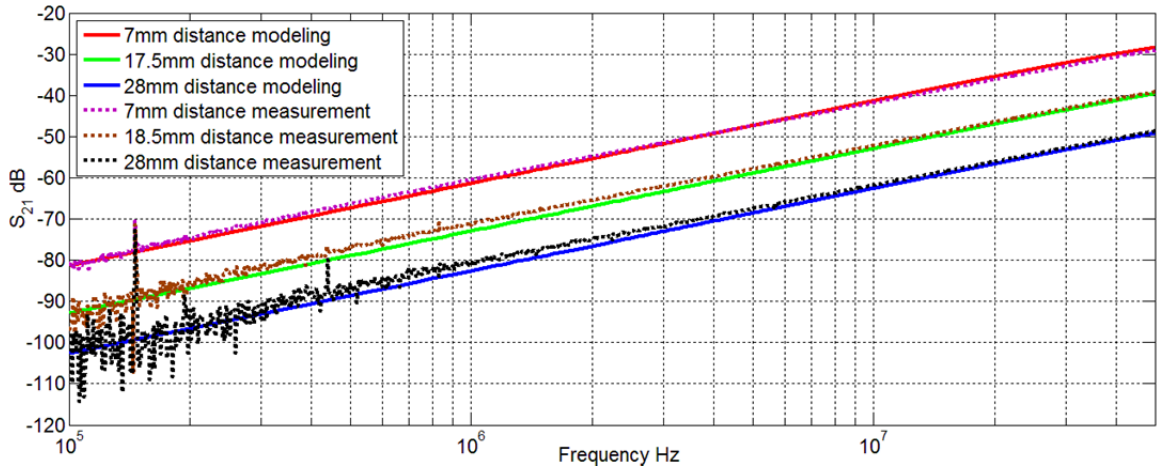


Fig. 5.26. Transfer characteristic of PCB2 with split track and capacitor model Cap3

5.4.4 Capacitor mutual inductance modeling

Capacitor mutual inductance can be modeled using 3D electromagnetic modeling tools available in the market, such as CST MWS. S-parameter measurements for two PCB prototype boards have been made- Fig. 5.20. (only PCB1 shown). These results are enough to extract the mutual inductance between two capacitors, if they are mounted in different distance from each other and if method, explained in Chapter 3.5, is used. Taking a look on results in Fig. 5.21. to Fig. 5.26. it can be concluded, that transfer parameter S_{21} changes, if distance between capacitors is changed, therefore it can be concluded that mutual inductance between capacitors is changing. Comparing the S_{21} for two PCB's, if the capacitors are in the same distance from each other, it can be concluded that PCB configuration has negligible effect on mutual inductance. As PCB configuration in this case has negligible effect on S_{21} parameter, it is obvious that it has negligible effect on mutual inductance, between two loops. Therefore, mutual inductance between PCB tracks at both ports is ignored and extracted mutual inductance using method described in Chapter 3.5, is assumed to be mutual inductance between two capacitors. Extracted mutual inductance results are presented in Fig. 5.27. and Fig. 5.28.

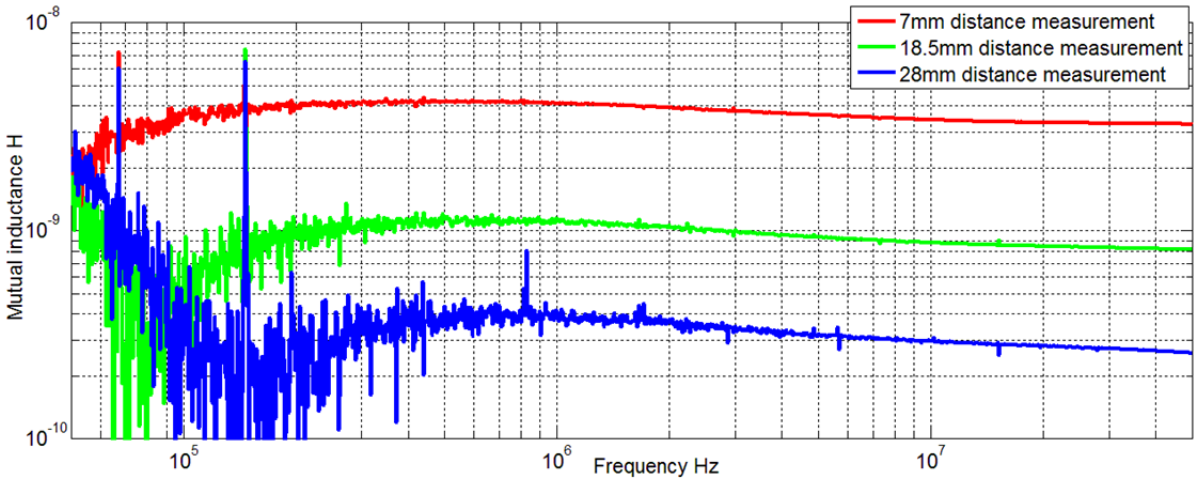


Fig. 5.27. Extracted mutual inductance between capacitors on PCB1 with different distances

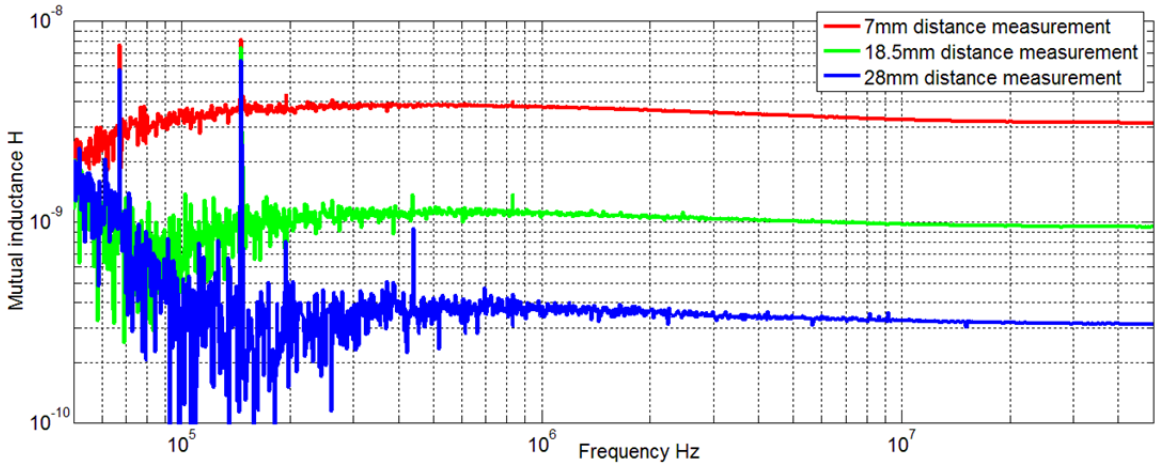


Fig. 5.28. Extracted mutual inductance between capacitors on PCB2 with different distances

Measurement results in the lower frequency range is quite noisy, due to the low energy levels to be measured, measurement equipment noise, floor and ambient noise (high peaks). Mutual inductance between two capacitors in the distance of 7mm at 1MHz is almost 4nH, in the distance of 18.5mm more than 1nH and in distance of 28mm almost 0.4nH. Mutual inductance has a slight drift over the frequency range, it can be explained by the measurement methodology and parasitic parameters not taken into account- such as connectors, connector connection etc. and measurement error.

Modeling results are compared with extracted results from measurements in Fig. 5.29. to Fig. 5.34. for both PCB types and three capacitor models- Cap1, Cap2, Cap3.

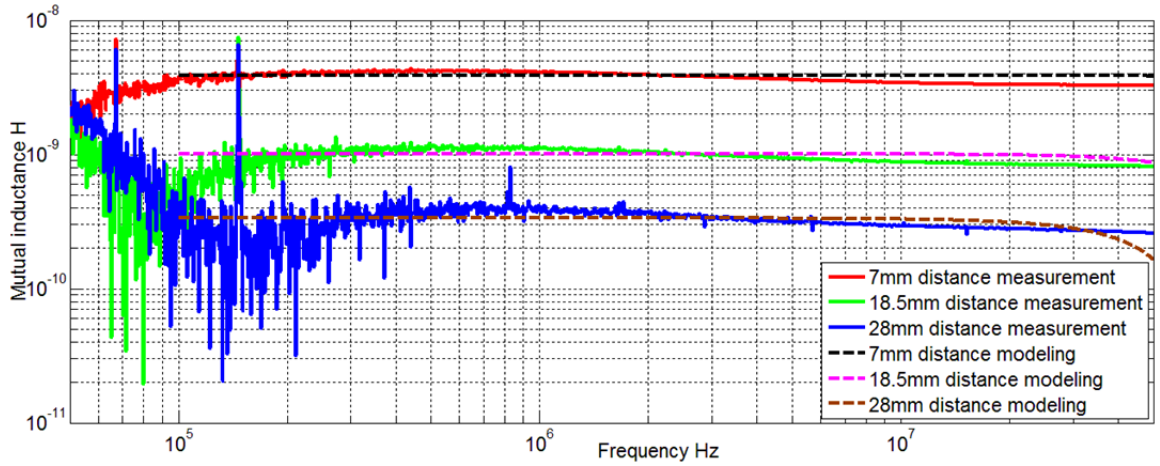


Fig. 5.29. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB1 with different distances for capacitor model Cap1

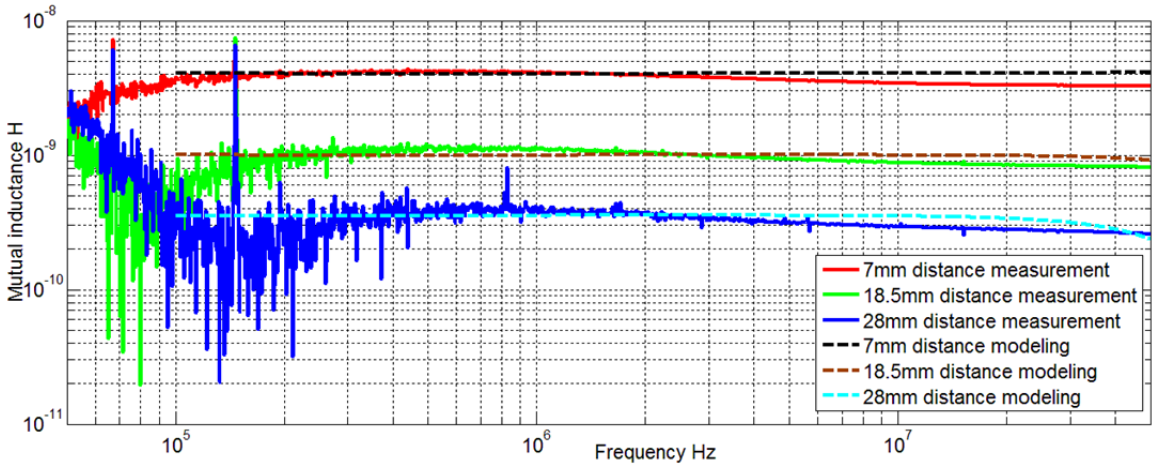


Fig. 5.30. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB1 with different distances for capacitor model Cap2

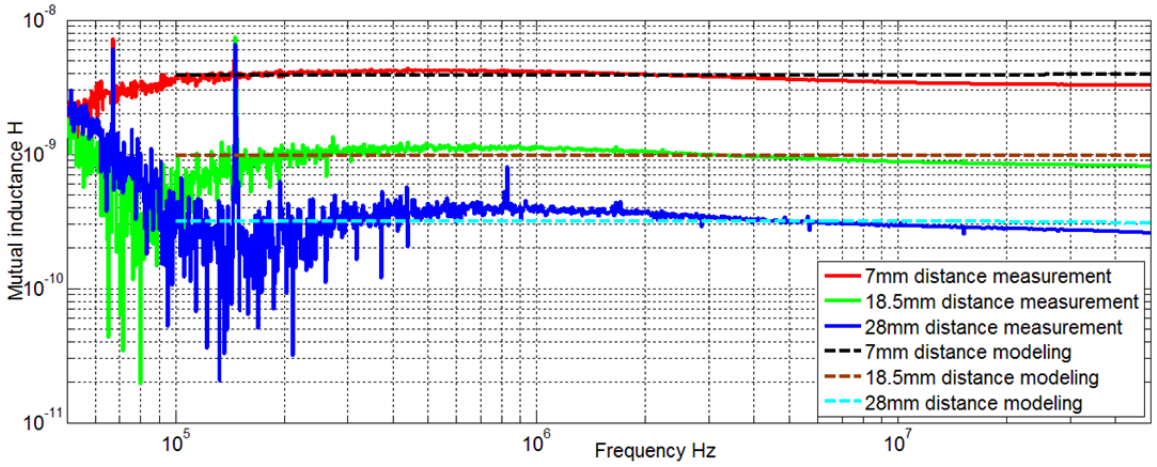


Fig. 5.31. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB1 with different distances for capacitor model Cap3

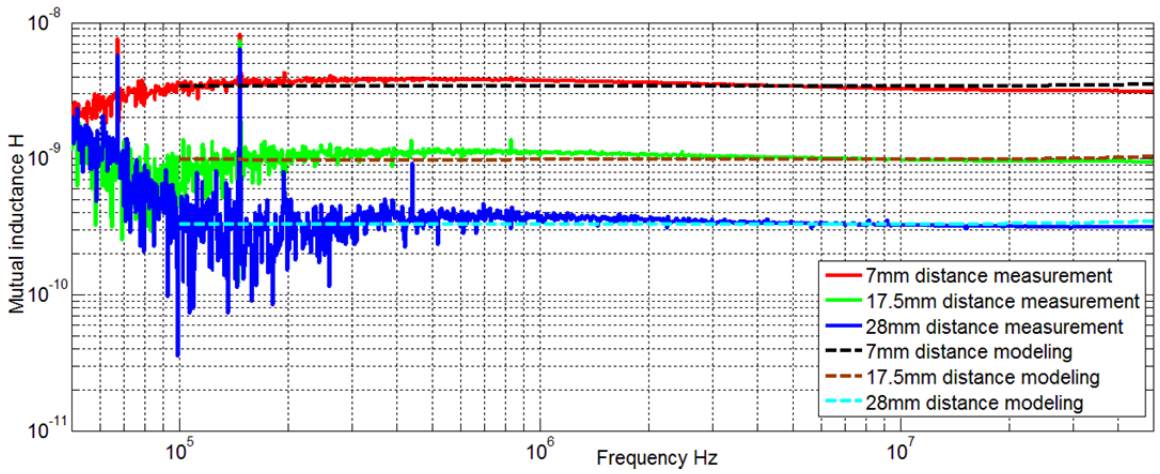


Fig. 5.32. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB2 with different distances for capacitor model Cap1

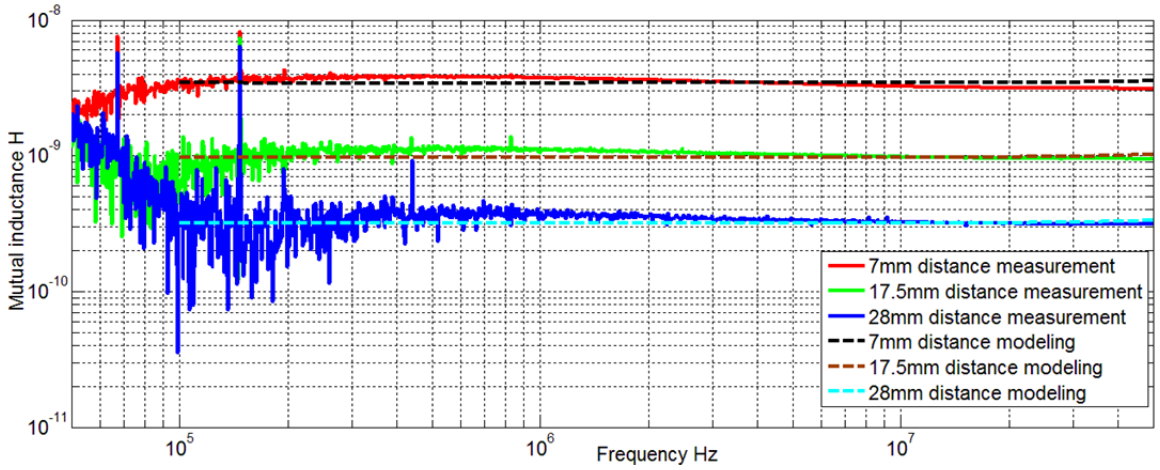


Fig. 5.33. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB2 with different distances for capacitor model Cap2

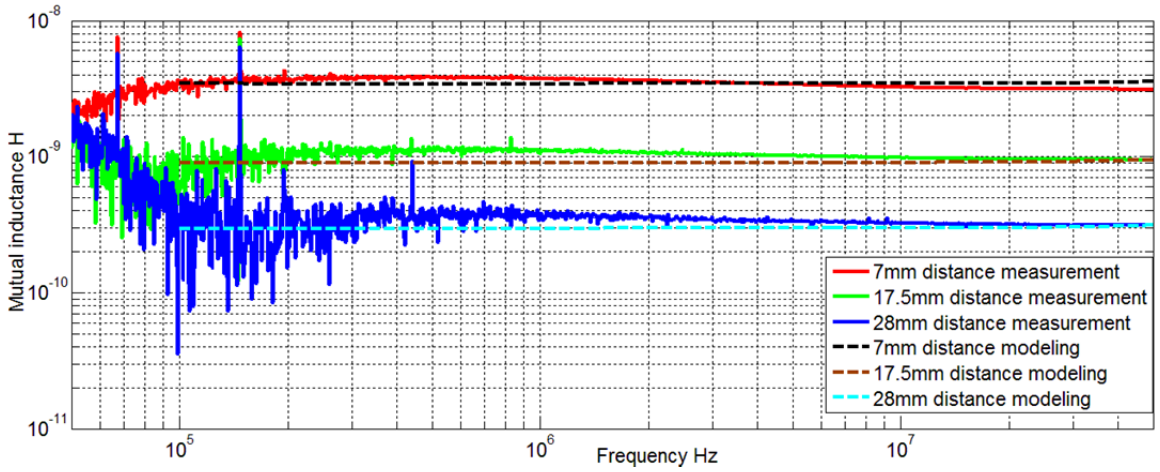


Fig. 5.34. Extracted mutual inductance from measurements and modeled mutual inductance between capacitors on PCB2 with different distances for capacitor model Cap3

All capacitor models- Cap1, Cap2, Cap3 with PCB1 and PCB2 give equally similar results and are very close to extracted results from measurements.

Mutual inductance dependence on distance between capacitors is analyzed using Cap3 capacitor models and PCB2 model in CST MSW modeling environment. It can be done also with other capacitor models and PCB1. Results are presented in Fig. 5.35. Mutual inductance decreases if distance between capacitors is increased.

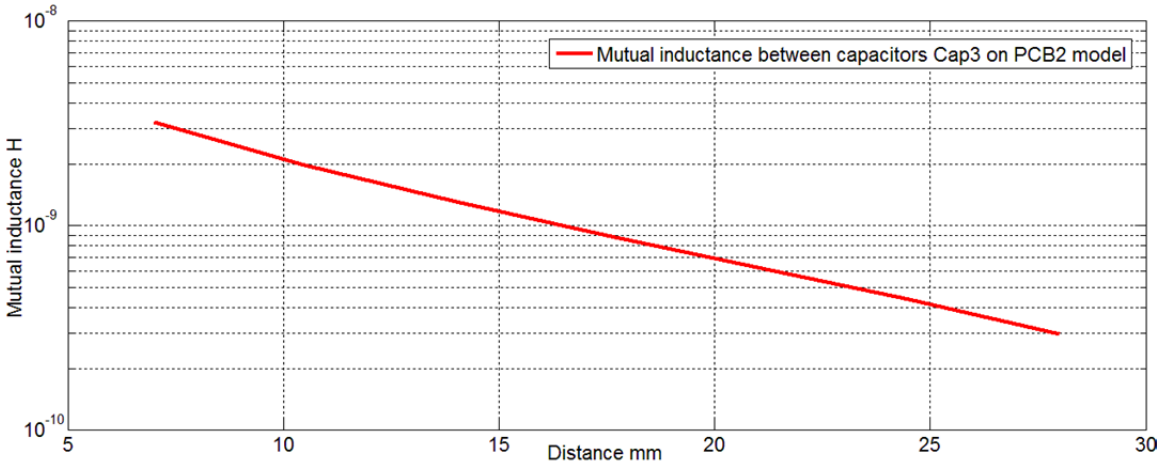


Fig. 5.35. Mutual inductance if capacitors are mounted in different distances from each other (modeling results achieved using Cap3 and PCB2 models)

5.5 Mutual inductance reduction techniques

Mutual inductance between capacitors is mainly created by the capacitor loops. One of the solutions is to reduce the capacitor created loop area. Mounting the capacitor as close to the PCB as possible gives positive result, but there is still a loop created by internal construction. This could be changed, if component manufacturers modified the component internal structure. But also this step has its limitations, due to insulation thickness between internal conductive parts and surrounding environment. Therefore, external add-ons, such as, ground plane on PCB and shielding, can be employed to reduce mutual coupling between capacitors. A shielding configuration between capacitors is proposed to reduce mutual coupling in Fig. 5.36. The shielding performance is evaluated by measuring transfer coefficient S_{21} and by modeling in CST MSW. For modeling capacitor models Cap3 have been used. The model is shown in Fig. 5.37. On top of PCB copper solid ground plane (GND) is added. Afterwards, copper shielding is added between capacitors. The connection and configuration of ground plane and shielding is extremely important. Measurements and modeling for various configurations have been made. Measurement results are shown in Fig. 5.38. Modeling results are compared with measurement result in Fig. 5.39. For modeling all conductive parts are modeled as PEC- perfect electric conductor, to reduce calculation time and memory usage.

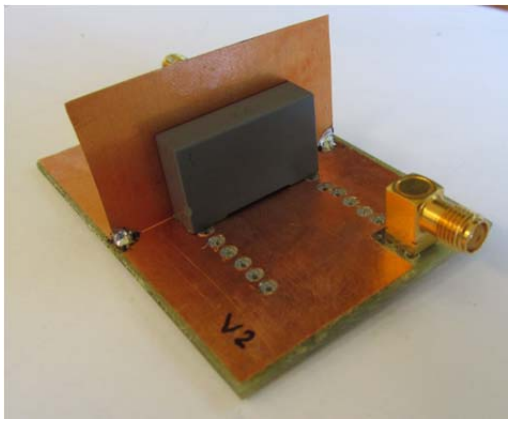


Fig. 5.36. Shielding configuration to reduce mutual coupling between capacitors with two connection points (soldered) between GND plane and copper shield

At first, PCB is measured without ground plane and shielding to have a reference. Then ground plane is added. During the measurement the ground plane is floating. In Fig. 5.38. it is clear, that ground plane increases coupling between two capacitors as transfer coefficient S_{21} increases by few dB. Then copper shielding is added between two capacitors, without soldering it to ground

plane. It should be noted that shielding material touches the ground plane of PCB, but doe to imperfections, it is not solid contact in full length. In Fig. 5.38., it is visible that coupling is reduced as transfer coefficient is reduced by 8dB. Further, shielding is soldered to ground plane at two and later at three points, as it is usually done in PCB fabrication, when thru hole mounting of shielding is used. Transfer coefficient decreases by 15dB to 17dB, thus reducing mutual inductance between capacitors. Finally, shielding is soldered along whole length to the PCB ground plane. Transfer coefficient reduces by more than 30dB. At frequencies up to 1MHz, transfer coefficient S_{21} is so low, that in Fig. 5.38. vector network analyzer noise is measured.

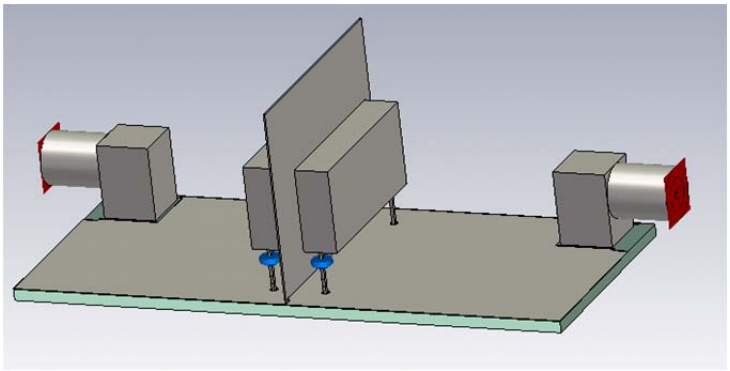


Fig. 5.37. Model for shielding evaluation between capacitors using Cap3 capacitor models

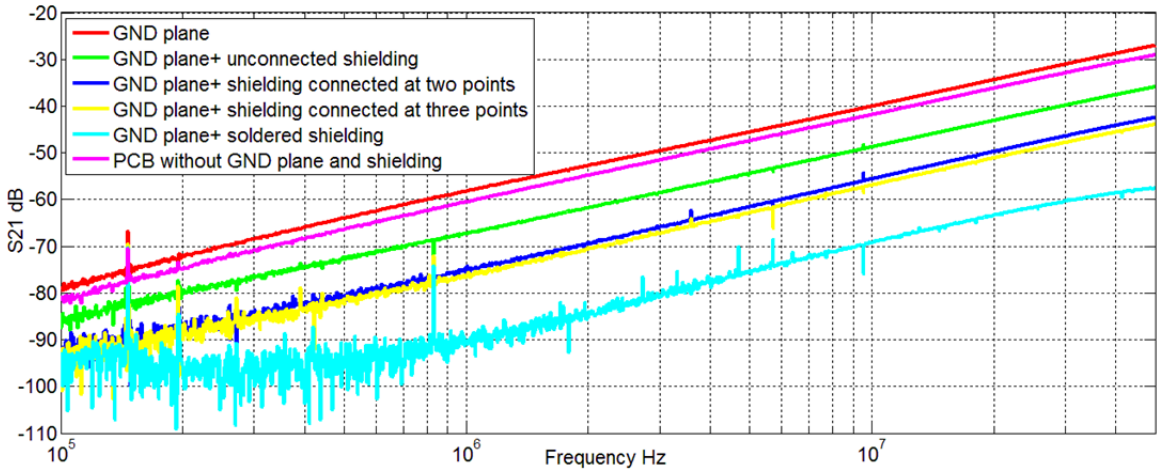


Fig. 5.38. Measurement results of various shielding techniques to reduce mutual coupling between capacitors

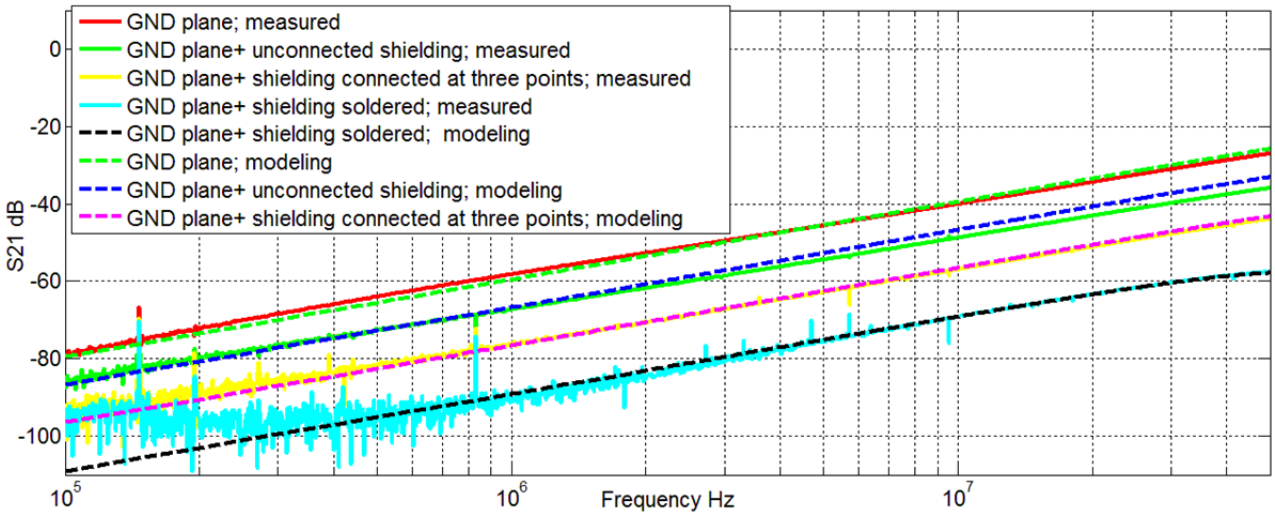
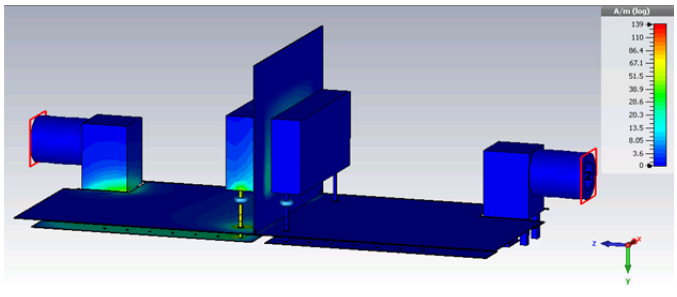


Fig. 5.39. Measurement and modeling result comparison of various shielding techniques to reduce mutual coupling between capacitors

The difference, when the shielding is connected in three or two points to ground plane and when the shielding is connected in whole length is huge, if transfer coefficient is measured. Therefore, with help of the surface current modeling in CST MSW the difference between two situations can be explained. If copper shield between capacitors is not connected in whole length, eddy currents are induced on both sides of shield due to the gaps in shielding, where the current can penetrate. If the copper shielding is soldered in whole length, the eddy currents have no gap to penetrate between two copper conductors. The situation is shown in Fig. 5.40. and Fig. 5.41.


a)

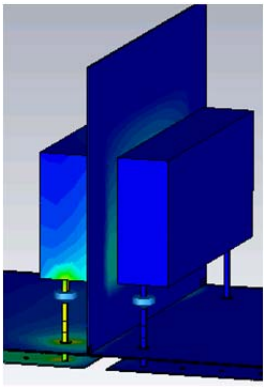
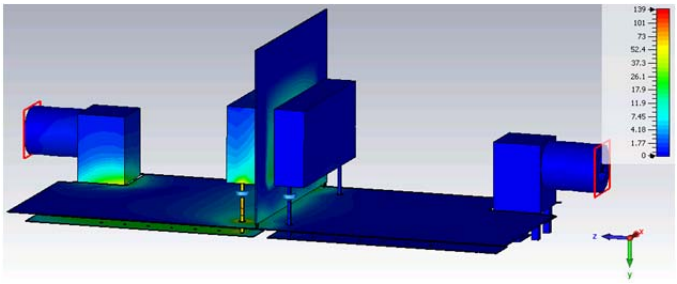

b)

Fig. 5.40. Surface current modeling results, if copper shield is connected in whole length. a) whole PCB, b) zoomed capacitors and shielding


a)

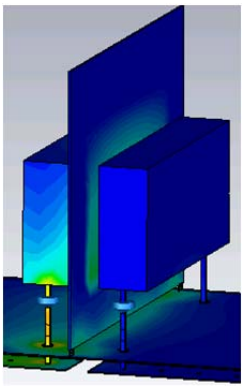

b)

Fig. 5.41. Surface current modeling results, if copper shield is not connected in whole length: a) whole PCB, b) zoomed capacitors and shielding

To directly analyze shielding configuration impact on mutual inductance between two capacitors, mutual inductance has been extracted from measurement results, Fig. 5.42. The

shielding with continuous connection to the ground plane has the best result, 12pH mutual coupling between capacitors at 1MHz. If shielding is connected at two or three points only mutual inductance increases up to 78pH and 61pH at 1MHz, respectively. If copper shielding is not connected at all but only placed between two capacitors the mutual inductance reaches 1.7nH at 1MHz. If no shielding and ground plane are used, the coupling is 3.7nH.

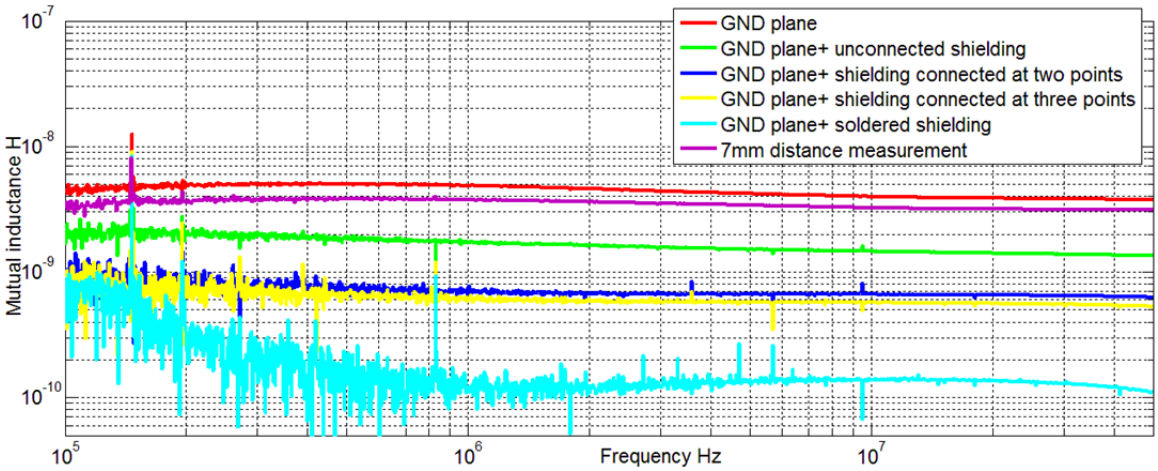


Fig. 5.42. Mutual inductance between capacitors with various shielding configurations

5.6 Conclusions

Capacitors can be modeled using 3D electromagnetic software tools available in the market. In this case modeling has been done using CST MWS. Three capacitor models have been proposed- Cap1, Cap2, Cap3. All proposed models during verification have shown that their performance is high enough to enable PCB mounted capacitor modeling and mutual inductance modeling between capacitors. Difference between three proposed capacitor models lays in their complexity that has direct impact on computational time and occupied memory. The first model- Cap1, has the most complex structure having curved faces and round connectors. Therefore, it represents in great details the real capacitor without outer insulation shell. Capacitor models Cap2 and Cap3 are created using rectangular shapes only that leads to lower mesh requirements and lower memory consumption, accordingly. Capacitor model- Cap3 has the lowest meshcell number and the lowest modeling time whatever solver is used and whatever mesh type is used. In all verification steps all capacitor models have shown that it is possible to model capacitors and their couplings to PCB and other capacitors with great accuracy. Therefore, all capacitor models can be used for this purpose. Capacitor model- Cap3 has at least 20% lower meshcell number in case if hexahedral mesh type is chosen, compared to capacitor model- Cap2 and at least 150% lower meshcell number compared to capacitor model Cap1. Capacitor model- Cap3 has at least 49% lower meshcell number in case if tetrahedral mesh type is chosen, compared to capacitor model- Cap2 and at least 400% lower meshcell number compared to capacitor model Cap1. Using both solvers and different mesh types it is obvious that Cap3 model calculation takes at least 30% less than Cap2 calculation and at least 250% less time than Cap1 calculation, if frequency domain solver with hexahedral mesh is used. For time domain solver the difference in calculation time is higher- Cap3 model calculation takes at least 16% less than Cap2 calculation and at least 1280% less time than Cap1model calculation. Capacitor model Cap3 is recommended to use in further EMI filter modeling.

Mutual inductance reduction techniques have been proposed, measured and modeled. Modeling results follow the measurement results very well and again prove that 3D electromagnetic field modeling can be successfully used in RFI filter modeling. Proposed shielding technique when copper shielding is soldered to ground plane in whole length reduces mutual coupling between capacitors from 3.7nH to 12pH at 1MHz. Other shielding techniques also reduce mutual coupling, but results are not so good. In case, if only ground plane is added on top of PCB to reduce mutual coupling between capacitors, the opposite result is achieved- mutual coupling is increased.

6. INDUCTOR MUTUAL INDUCTANCE MODELING

6.1 Background

In EMI filter, components such as inductors, often are mounted next to each other as close as possible to save space, leading to mutual couplings [17] that degrade the filter performance. There have been various measurement techniques for mutual coupling measurements presented [49], [17], extraction [50], mutual coupling reduction [51] and optimization [18], [19], [20], already discussed in previous chapters. Previous chapter gives an overview on capacitor-capacitor mutual coupling modeling. There is lack of information on techniques and possibilities, using, in the market available, the most popular 3D electromagnetic modeling tools that could help in more effective manner to solve problems related to inductor-inductor mutual coupling. However, there are some articles that have described 3D electromagnetic modeling tools in EMI filter modeling [21], [22], [23], but these are not the industry driven 3D electromagnetic modeling tools. In this chapter there is EMI filter inductor modeling and inductor-inductor mutual coupling modeling proposed, using CST MWS.

6.2 Prototype PCB for measurements and modeling

Two prototype PCB's have been created, for inductance and mutual inductance measurements. The first PCB board is created to measure PCB mounted inductor parameters. One SMA connector is added to enable S-parameter measurements that afterwards can be converted to Z-parameters. PCB prototype and its 3D model are shown in Fig. 6.1. Reflection coefficient measurement method is used for first PCB. Reflection coefficient measurement methodology and measurement error is discussed in Chapter 2.7.

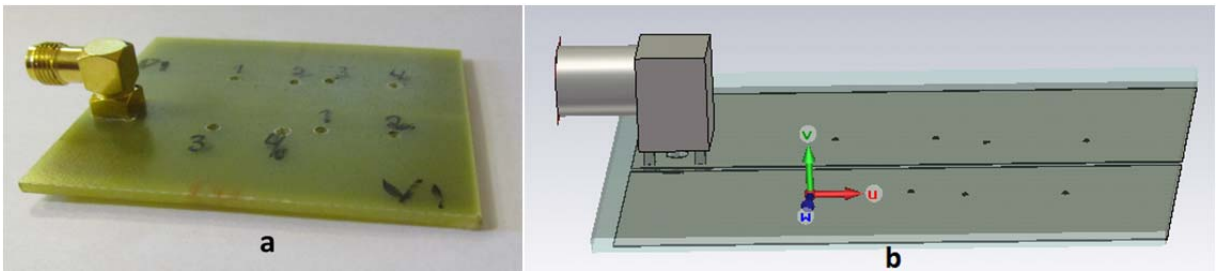


Fig. 6.1. a) PCB prototype for inductor measurements, b) PCB 3D model for modeling in CST MSW

Second PCB is developed to measure mutual coupling between two inductors. Two SMA connectors are used to measure S-parameters. PCB prototype and 3D model is shown in Fig. 6.2.

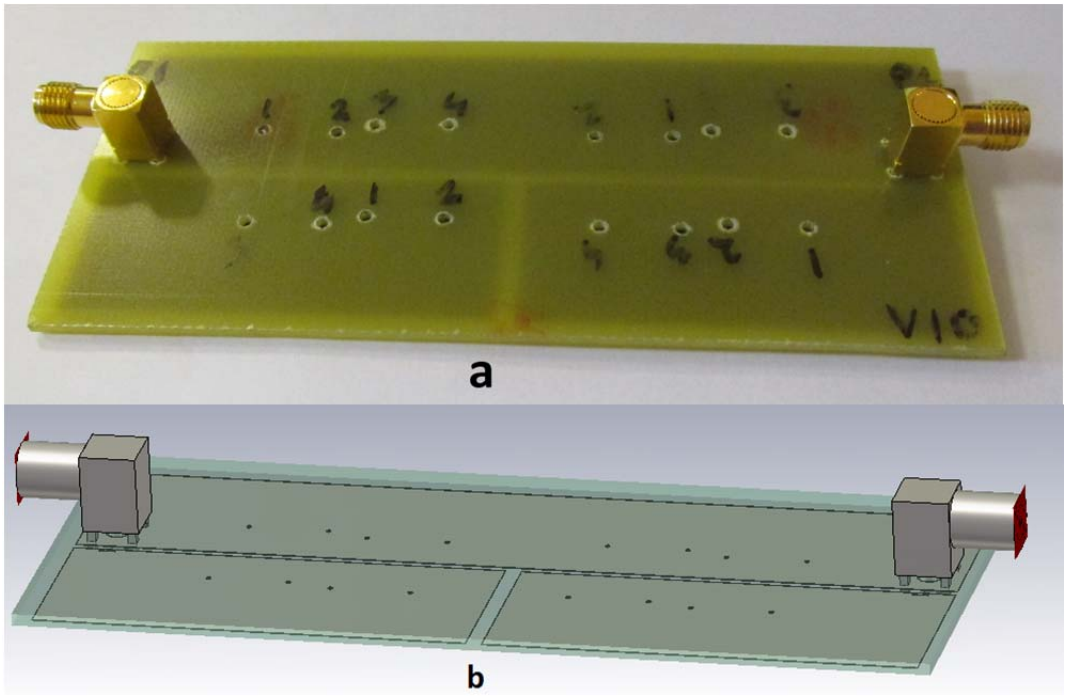


Fig. 6.2. a) PCB prototype for mutual inductance measurements between inductors, b) PCB 3D model in CST MSW

Models of both prototypes are created in CST MWS [54]. PCB board insulation material is FR4 (loss free). All conductive parts of both models are modeled as PEC- perfect electrical conductor. The insulator for SMA type connector is Teflon (PTFE) (loss free). All 3D model materials are chosen from default material library without any parametric modifications.

Using second PCB, we are interested to extract mutual inductance between two inductors mounted on it. Therefore, second PCB is modeled without components, creating high impedance termination for both SMA ports. If inductors are mounted on PCB, they create high impedance

termination for both SMA ports, rather than low impedance termination. This is the main reason why open circuit modeling and measurements are done instead of short-circuited modeling and measurements for verification purposes. Results are presented in Fig. 6.3. as forward transfer coefficient- S_{21}. Measurement results and modeling results agree very well in whole frequency range.

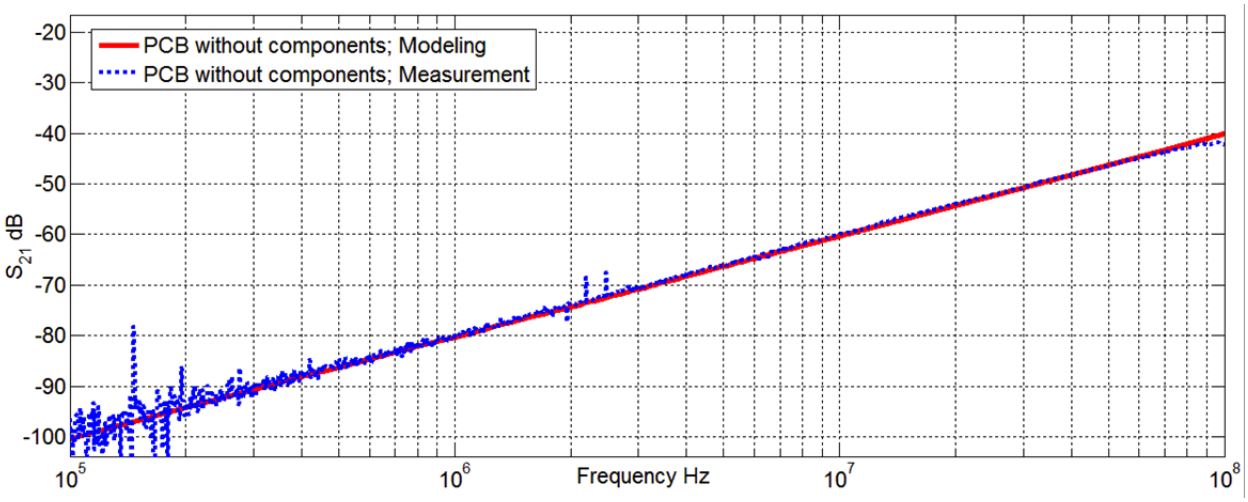


Fig. 6.3. Measurement and modeling results of PCB without components

Using extraction techniques described in Chapter 3.5., coupling impedance can be extracted between two SMA ports. Extracted impedance form measurement and modeling results are presented in Fig. 6.4. and impedance angle in Fig. 6.5. Impedance has capacitive character if frequency is higher than 1MHz, as impedance phase angle is negative. From impedance measurements and modeling results in Fig. 6.4., capacitance can be calculated. Measurement results yield 11,5pF, but modeling results 63,1pF at 10MHz. Impedance extracted from measurement and modeling results do not agree at all, despite the fact that modeled forward transfer coefficient S_{21} predicts measured S_{21} with high accuracy in Fig. 6.3. Impedance and impedance angle are calculated using equation (2-47). Impedance and impedance angle depend not only on transfer coefficients, but also on reflection coefficients. Measured and modeled transfer coefficients S_{21} and S_{12} agree very well, S_{12} are not shown in Fig. 6.3.

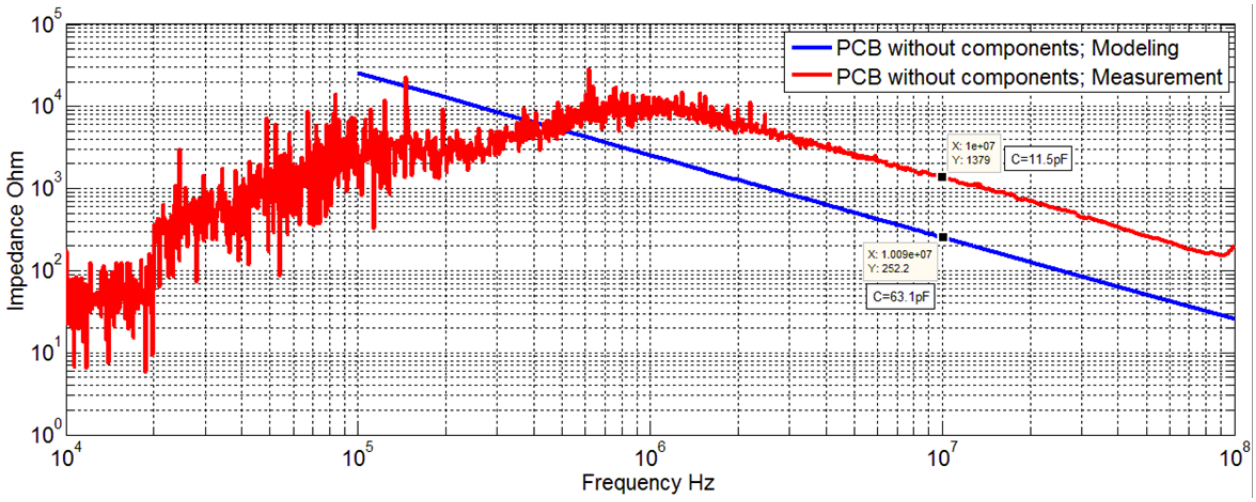


Fig. 6.4. Extracted coupling impedance between two SMA ports on second PCB

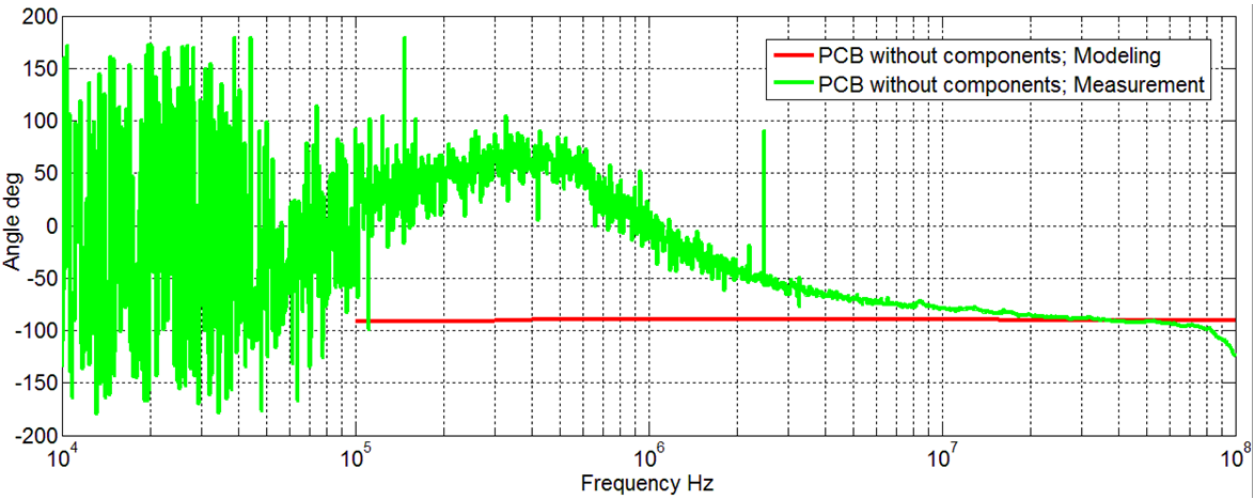


Fig. 6.5. Extracted coupling impedance angle between two SMA ports on second PCB

In Fig. 6.6 there are modeled and measured reflection coefficients presented. Modeling results predict 0dB reflection in whole frequency range as measured PCB is unloaded (open circuit). Measured results yield slight difference from modeled results up to ~30MHz, and quite large difference at 100MHz. In case of reflection coefficient angle, measurement and modeling results do not comply in frequency range higher than couple MHz. Difference between measured and modeled reflection coefficient can be explained by increased measurement error of vector network analyzer measuring reflections from high impedance ports, as described in Chapter 2.6. and Chapter 2.7. Although, the error is not high and measured reflection coefficients have only slight differences in respect to modeled results, it is enough to create large difference if impedance is calculated using equation (2-47) from measured and modeled results. Equation

(2-47) result is very sensitive to small deviations of reflection coefficient. Therefore, this is the main reason in impedance result differences in Fig. 6.4. and Fig. 6.5. This explains also why impedance angle at up to 1MHz is positive, yielding inductive impedance characteristic, while modeling predicts purely capacitive impedance characteristic.

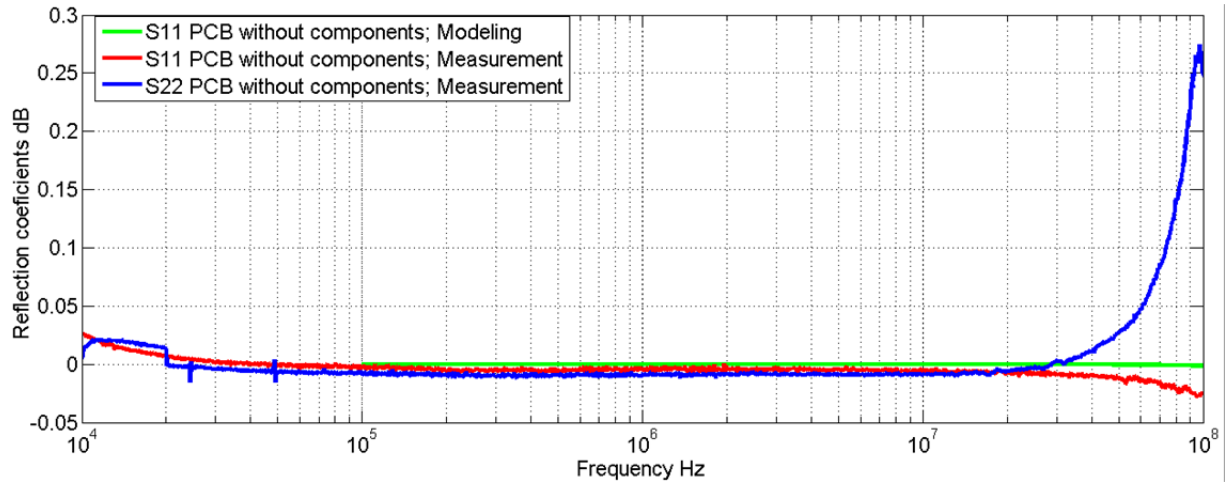


Fig. 6.6. Modeled and measured reflection coefficients of second PCB without inductors

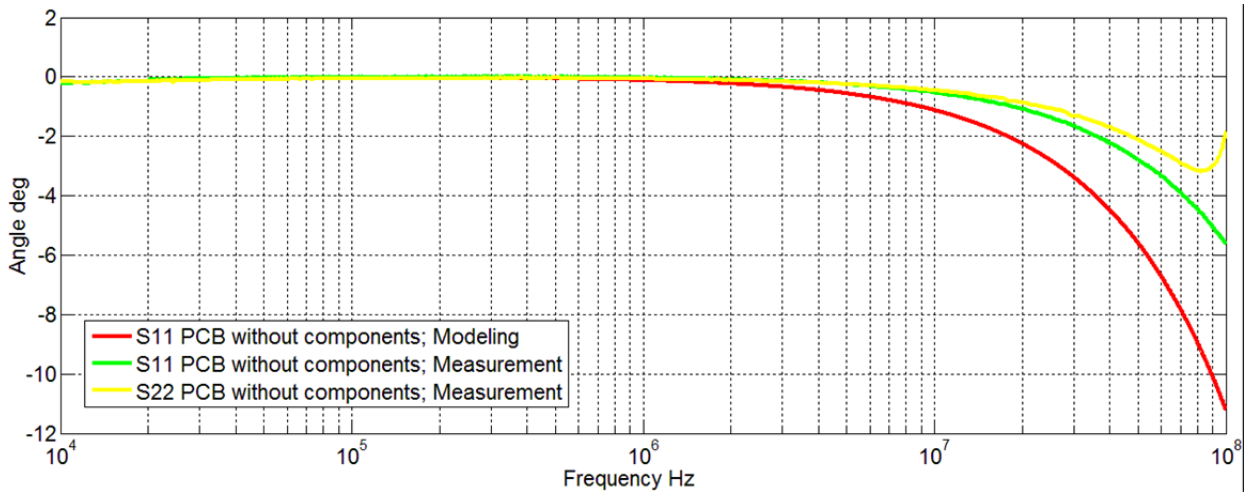


Fig. 6.7. Modeled and measured reflection coefficient angles of second PCB without inductors

6.3 Inductor modeling and verification

Conventional inductor is made from couple of windings on core, made from magnetic material or nonmagnetic material. Characterization of inductor with toroid core is complex and time consuming task. Inductor parasitic parameters depend on physical dimensions of inductor components- core material, core size, core insulation thickness, winding wire diameter, winding

wire material and insulation thickness, winding turn spacing and winding turn count. Inductor inductance L depends on core material characteristic, winding turns count and distance between core and winding. Parasitic capacitance- EPC depends on distance between windings and distance between core and windings, including coating material properties of core and winding.

For measurements inductor core is chosen from Wurth Elektronik. Wurth Elektronik has provided precise magnetic material characteristics- conductivity and complex magnetic permeability. Inductor is shown in Fig. 6.8.a. Inductor contains 36 turns winded on toroid core with inner diameter 12mm outer diameter 26mm and core height 16mm. For 3D electromagnetic modeling inductor model is created. The model is created with ferrite toroid core, including winding with 36 turns, Fig. 6.8.b. In 3D model winding insulation is not modeled, as it will increase mesh cell count drastically, due to the reason that insulation is very thin layer in comparison to other dimensions of inductor. It is possible to create new materials in CST MWS with frequency dependent characteristic as CST MWS is very flexible modeling packet. Therefore, information provided by Wurth Elektronik can be implemented in toroid core material model. Toroid core coating is not modeled also, as it will increase mesh cell count drastically, for the same reasons as winding insulation modeling. As the ferrite material is a dispersive material (permeability is frequency dependent) it is possible to use only frequency domain solver. Time domain solver does not support dispersive materials. To decrease complexity of inductor model, winding material is defined as PEC- perfect electrical conductor. As we are not interested in DC characteristic and copper losses, copper substitution with PEC will give negligible effect on modeling results.

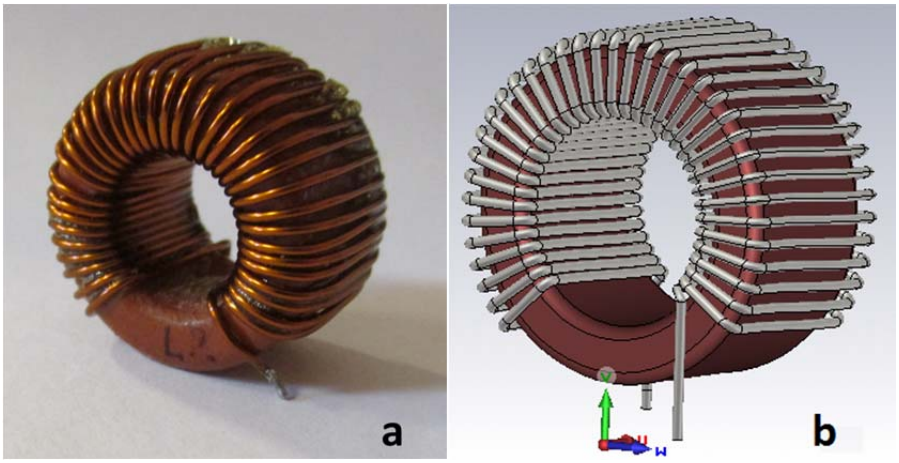


Fig. 6.8. a) Measurement prototype inductor, b) CST MSW 3D model of inductor

To verify PCB and inductor interaction, inductor is placed on PCB in two different positions and rotated by 90^0 degrees. All four positions are shown in Fig. 6.9. Two identical inductors are measured.

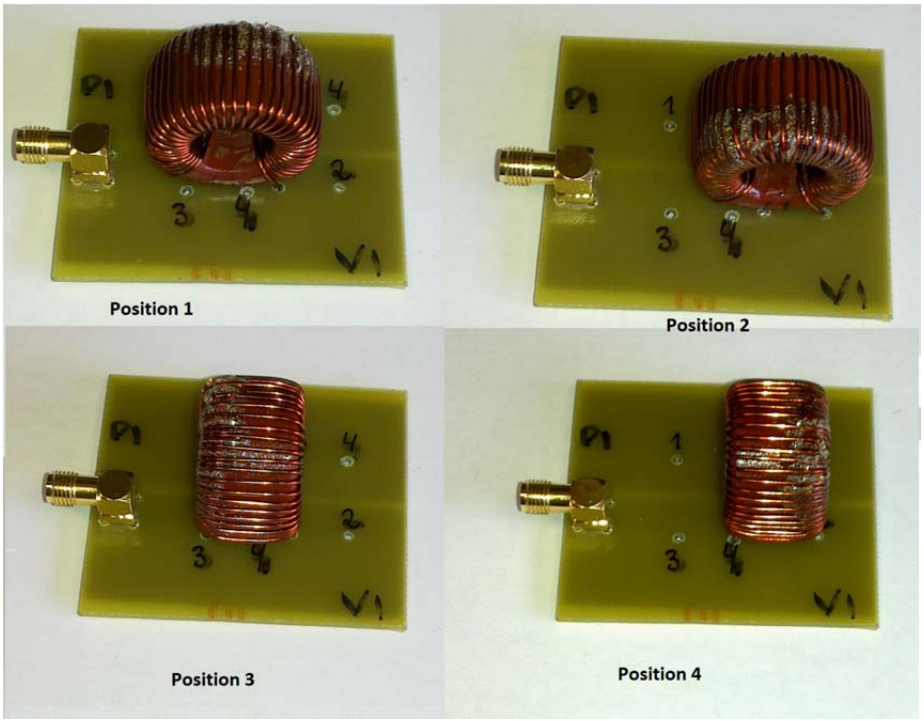


Fig. 6.9. Positions of inductors during measurements

Impedance measurements are carried out for both inductors in all four positions. In Fig. 6.10 inductor L1 inductance is presented for all positions. Impedance is not changing its characteristic when inductor is moved from position 1 to position 4. Therefore, it can be concluded that PCB and inductor interaction give negligible impact on inductor impedance.

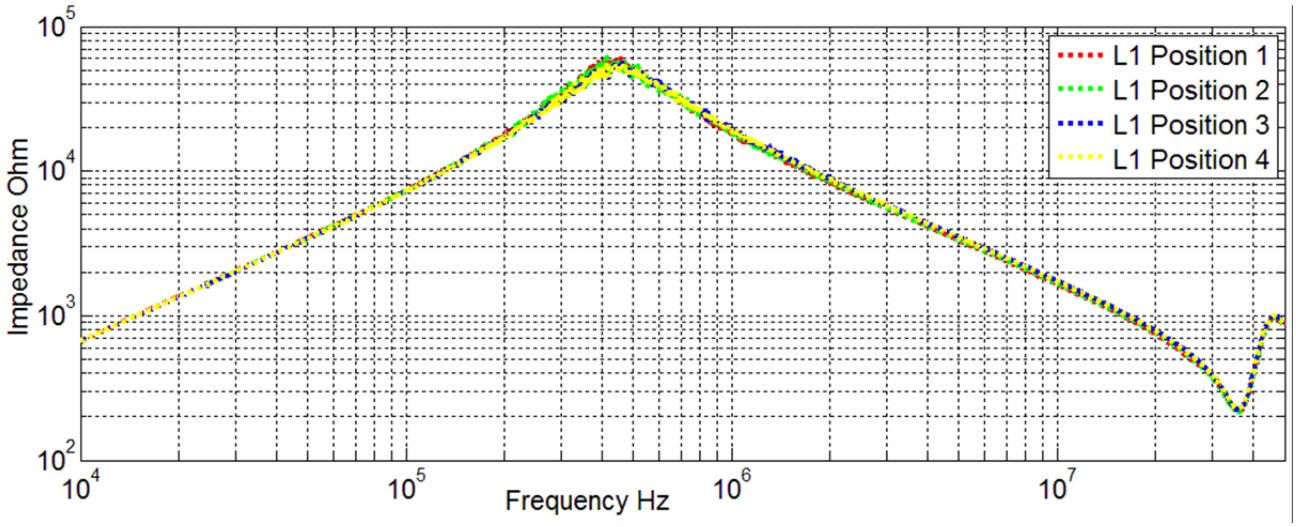


Fig. 6.10. Inductor L1 impedance measurements in four positions

The same situation can be observed with inductor L2, position of inductor has negligible impact on impedance. It should be pointed out that both inductors L1 and L2 are made from identical materials and physical dimensions are the same, but impedance of both inductors is not exactly the same. It can be explained by the fact that both inductors are not manufactured identically and have tiny differences, such as- winding turn to winding turn distance, winding turn to core distance. The deviation of inductance is shown in Fig. 6.11., for position 1, for both inductors- L1 and L2.

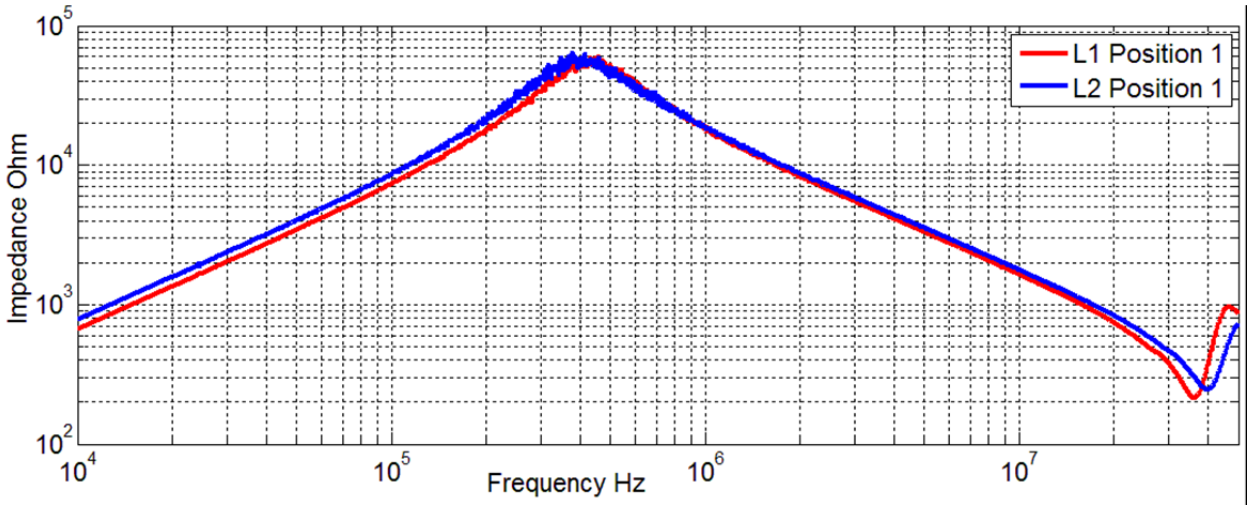


Fig. 6.11. Inductor L1 and L2 impedance in position 1

Modeling results in CST MSW also give similar results- position of inductor has negligible impact on impedance. Modeling results are presented in Fig. 6.12., for all four inductor positions. In low frequency range 10kHz-100kHz CST MWS do not give results with high

accuracy as the model is optimized to deliver precise results in high frequency range. It is possible to optimize the model to deliver more precise results in lower frequency range (up to 100kHz), but in this case the higher frequency range precision will suffer or modeling time will increase.

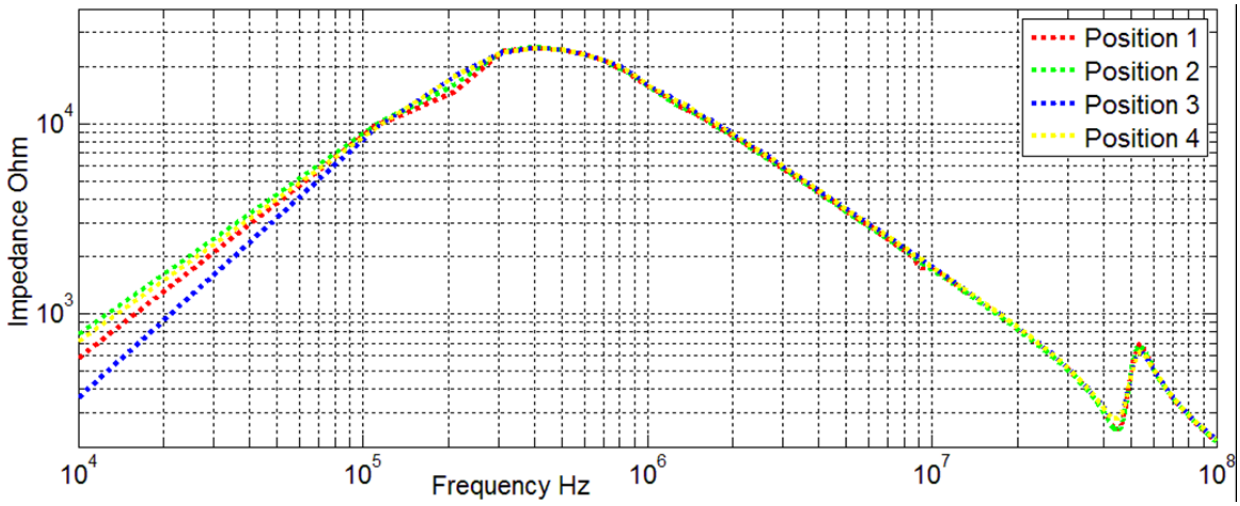


Fig. 6.12 Inductor impedance modeling results in CST MWS

In Fig. 6.13 modeling results with inductor 3D model are compared with measurement results for inductor position 1. Modeling results fit the measurement results quite well, except the first resonance depth and second resonance frequency. At first resonance frequency CST MWS predict impedance much lower than measurements. The measurements claim 60kOhm while modeling gives 25kOhm impedance at 410kHz frequency.

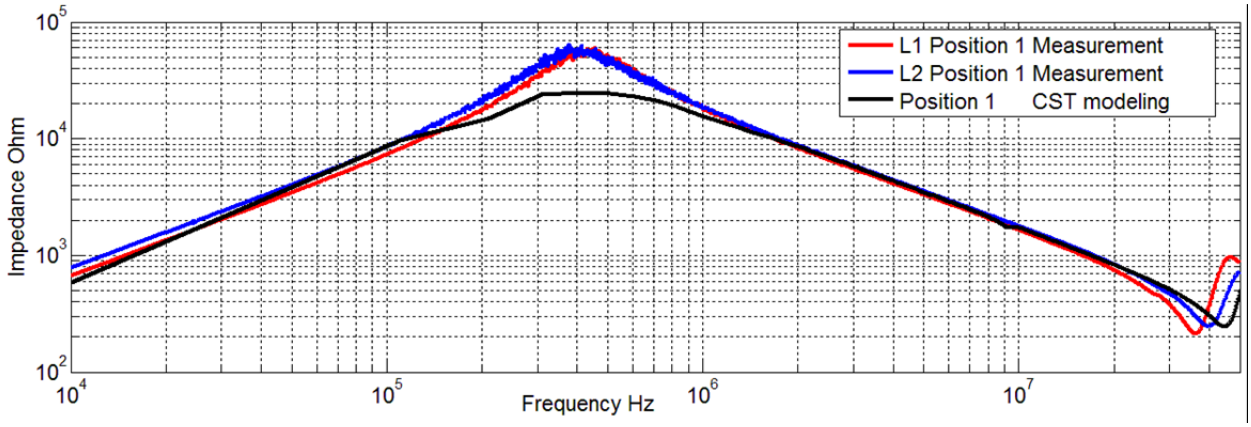


Fig. 6.13. Inductor impedance modeling using inductor 3D model and measurement result comparison

This error is connected to modeling mesh density in the volume between toroid core and winding turns. If mesh density is increased, it is possible to achieve better result fitting, but it dramatically increases the modeling time. The second resonance (at 30-50MHz) is also connected with the mesh density between toroid core and winding turns and 3D model slight inaccuracies.

To verify that the inductance can be properly modeled, it has been calculated from impedance measurements and CST MSW impedance modeling results. Results are presented in Fig. 6.14. Despite the fact that mesh is not optimized for low frequency modeling, the modeling and measurement inductance results agree quite well in the linear impedance range, 10kHz-100kHz. Close to the resonance frequency the inductance calculation using impedance modeling and measurement results is not correct, therefore it is obvious that close to the resonance the frequency inductance has not linear characteristic.

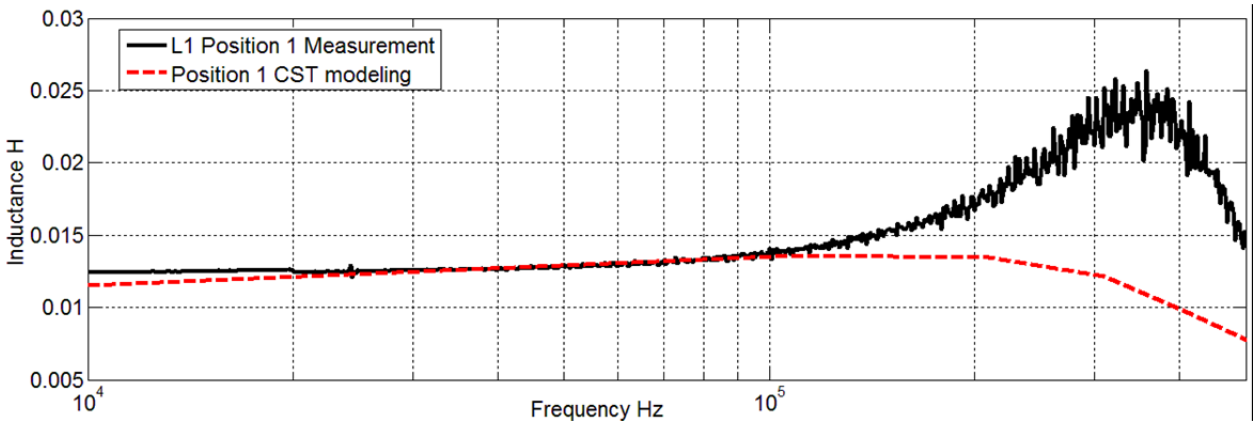


Fig. 6.14. Inductor L1 inductance comparison- CST MSW modeling, measurement

6.4 Mutual coupling modeling between inductors

Afterwards inductor model is verified and the impedance measurement and modeling results agree well, mutual coupling between two inductors can be modeled. For measurements, PCB prototype board, shown in Fig. 6.2., is used. Two inductors shown in Fig. 6.8 are mounted in three different positions and in two different distances from each other. All three positions are shown in Fig. 6.15. where inductors are positioned in 30mm distance from each other (distance is measured from toroid core center). A situation also is modeled and measured, if the inductors are positioned in 55mm distance from each other. Prototype PCB is connected to two port vector network analyzer and S-parameters are measured. The coupling between two inductors results in

change of S_{21}- forward transfer coefficient. Measurement results compared to modeling results are presented in Fig. 6.16. to Fig. 6.18. Measurement results show that there is a small difference in S_{21} (few dB), between two distances- 30mm and 55mm. Measurement and modeling results agree very well, even the resonances are modeled quite well in frequency range 20MHz-60MHz. To evaluate which inductor position delivers the worst coupling, the measurement results are regrouped in Fig. 6.19. PCB measurement results without inductors mounted on it are included in Fig. 6.19. as a reference. It appears that there is a little difference between transfer coefficients S_{21} of all three positions. Position 3 has the highest coupling, but it is only by 3dB higher than position 1 transfer coefficient, that appears the worst coupling result. PCB without components provides only by 3dB lower coupling than position 1.

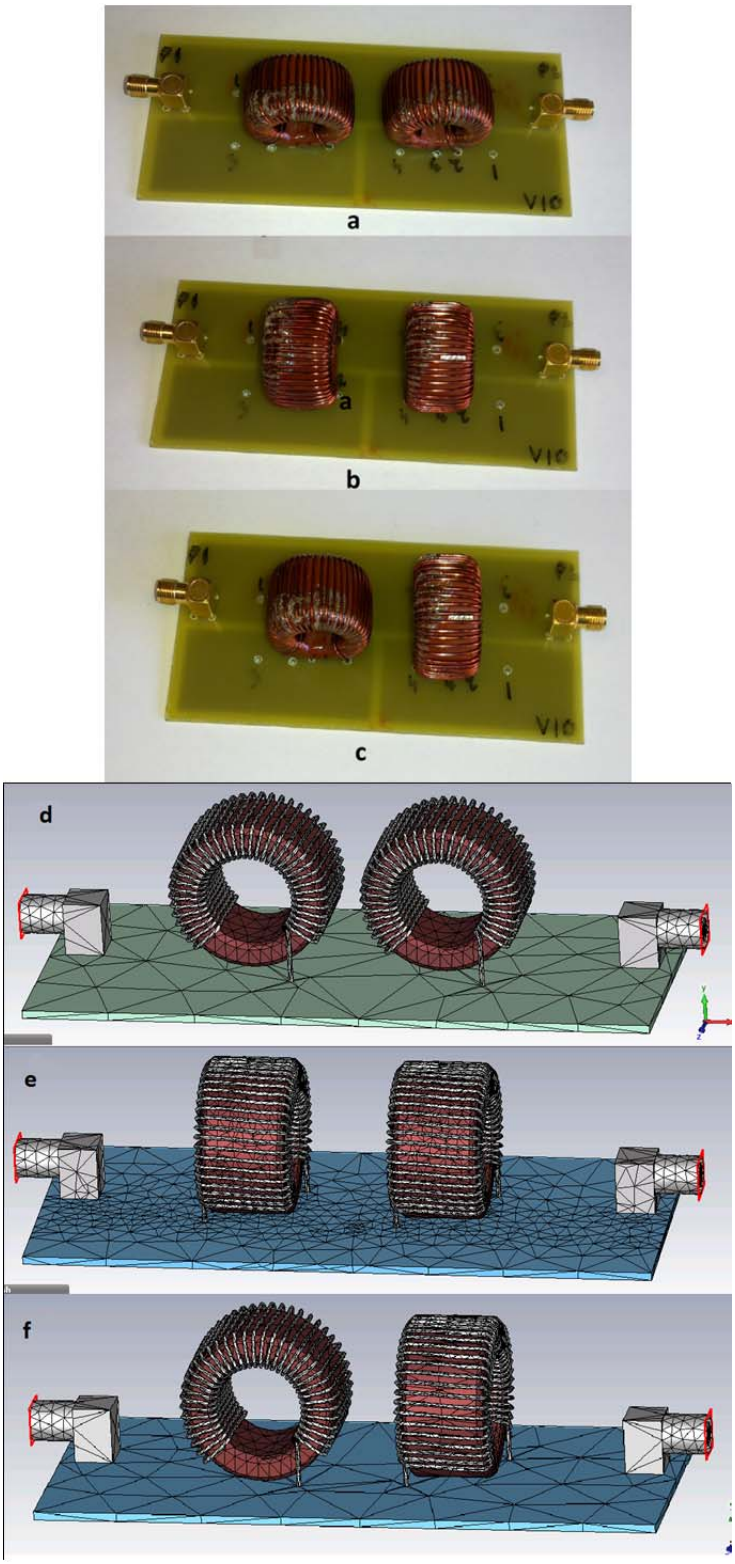


Fig. 6.15. Three different positions of inductors, if distance between them is 30mm: a) Position 1, prototype, b) position, prototype 2, c) position 3, prototype, d) position 1, 3D model, e) position 2, 3D model, f) position 3, 3D model

These results are not in contrary to recommendations in literature [56] and other that components aligned perpendicularly creates lower coupling. In case of used inductors, component leads are spaced in the way that rotation of component does not considerably change the cross section area in plane between two inductors. Interaction between inductors is mainly due to mutual coupling created by inductor lead formed loops. It should be noted that reason of measurements and modeling was not to discover optimized positioning of inductors on PCB, but to verify the possibility of CST studio usability in mutual coupling modeling between two inductors on PCB.

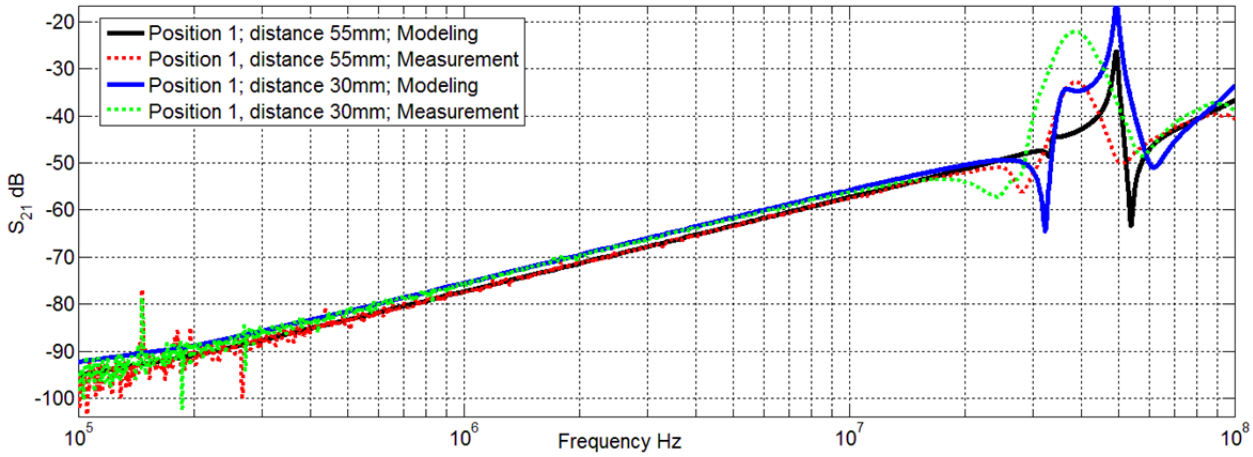


Fig. 6.16. Coupling measurement results and modeling result comparison between two inductors placed in position 1

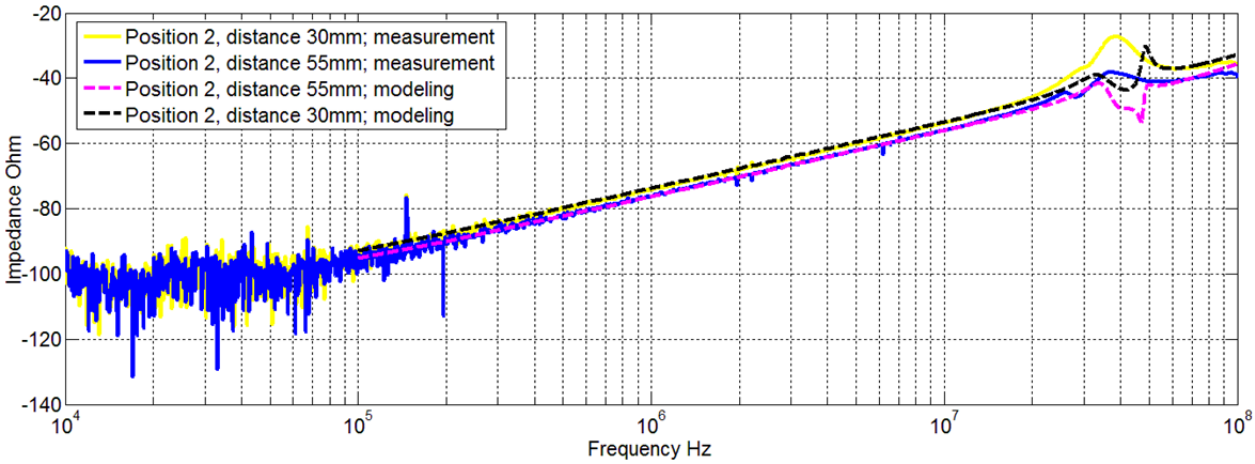


Fig. 6.17. Coupling measurement results and modeling result comparison between two inductors placed in position 2

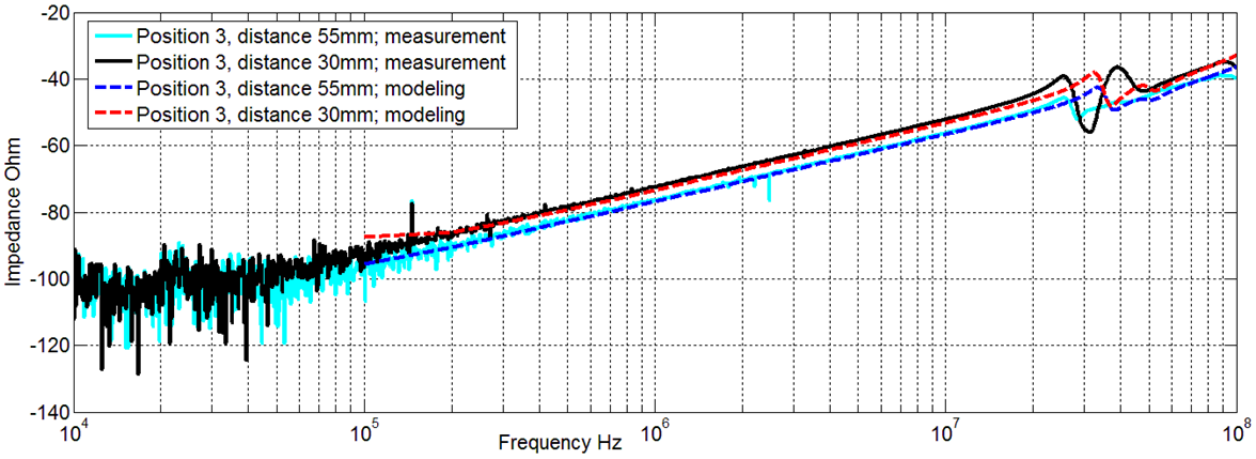


Fig. 6.18. Coupling measurement results and modeling result comparison between two inductors placed in position 3

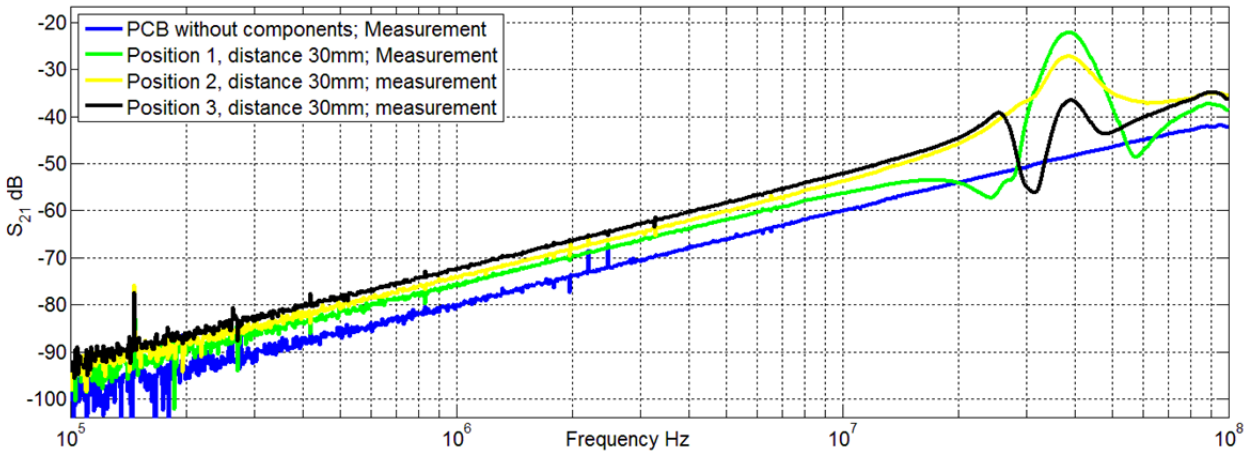


Fig. 6.19. Coupling measurement results between two inductors placed in position1, position 2, position 3 in 30mm distance

Mutual coupling between two inductors can be analyzed in sense of impedance. If calculation methodology is used as defined in chapter 2, exploring measured circuit as two port T-type network and applying equation (2-48), coupling impedance can be calculated in frequency domain. Impedance is calculated for Position 1, when inductors are positioned in 30mm distance using measured S-parameters and S-parameters acquired by modeling. Impedance results are compared in Fig. 6.20. Calculated impedance acquired by measuring and modeling results fits quite well in whole frequency range, except near ~30MHz, where impedance resonance is not modeled very accurately. It appears that impedance is not purely inductive as it is calculated in the case represented in chapter 3.5 and results represented in Fig. 3.20. To verify the impedance

characteristic, impedance phase angle is calculated for both- measured and modeled results and represented in Fig. 6.21.

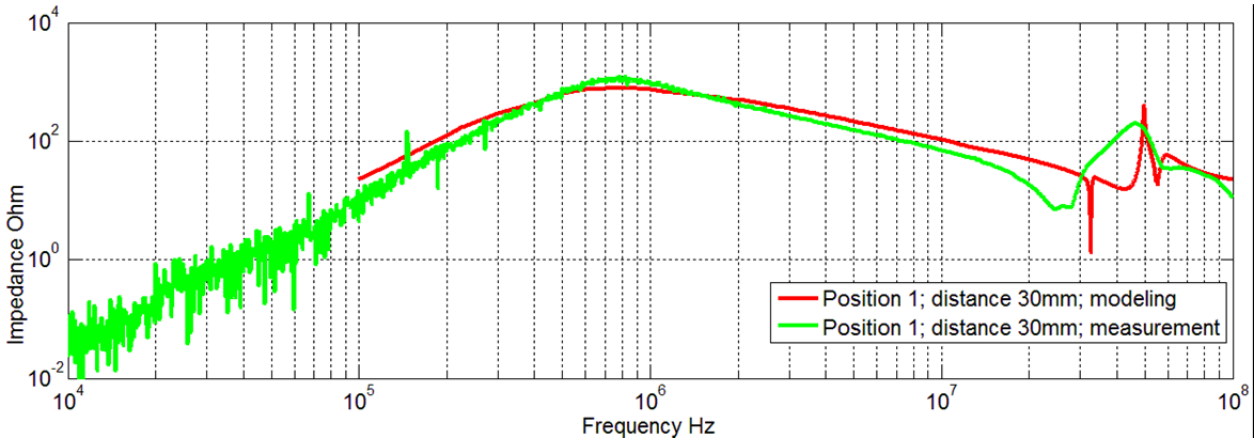


Fig. 6.20. Mutual coupling impedance in Position 1; 30mm distance

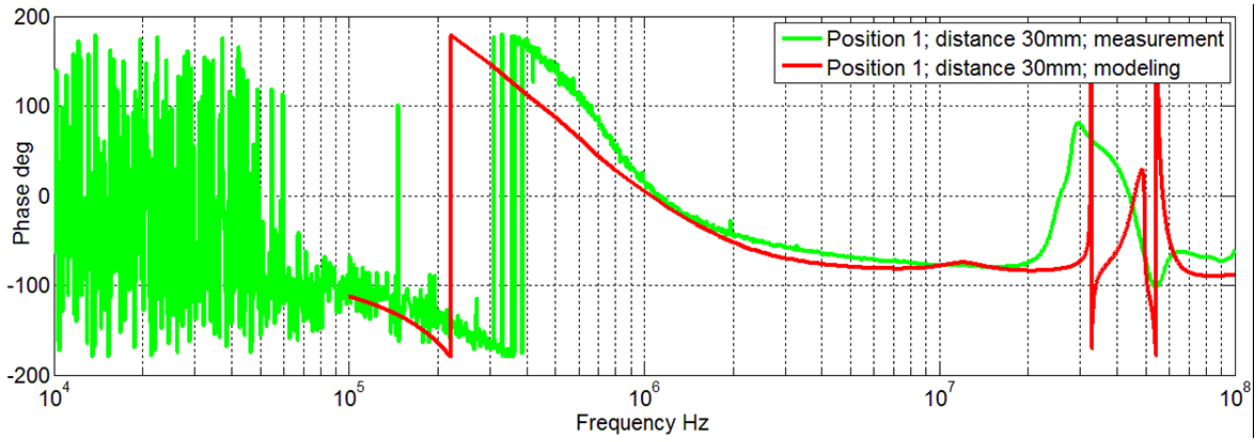


Fig. 6.21. Mutual coupling impedance angle in Position 1; 30mm distance

Measured and calculated impedance phase angle results agree quite well, except at 30MHz range where impedance resonances appear and in kHz range where abrupt phase switching occurs. Measurement results are noisy at the very beginning of measurements. Phase angle higher than $|90^0|$ could be explained by the fact that circuit acts as transformer in frequency range up to 50kHz. Up to 1MHz impedance performs inductively. In frequency range 1MHz-20MHz impedance has capacitive character. Afterwards couple of resonances occurs with abrupt phase changes. Therefore, it can be concluded that coupling between two inductors has mutual inductance and parasitic capacitance in parallel, as in Fig. 6.20. a parallel resonance is represented. Parasitic capacitance can be explained by the fact that PCB has its self-parasitic capacitance, already examined in Fig. 6.4. If inductors are placed on PCB, extra stray

capacitance is added. Capacitance in frequency range 1MHz-10MHz is calculated and presented in Fig. 6.22. for both- measurement and modeling results, as in this frequency range Xc is dominating. Capacitance is calculated using equation (2-77). It appears that calculated capacitance is well predicted by the modeling results. In the same manner inductive impedance component can be calculated in impedance range where X_L is dominating, using equation (6-1). Calculated inductive component results are presented in Fig. 6.23. Calculated inductance results from measured and modeled S-parameter results agree very well.

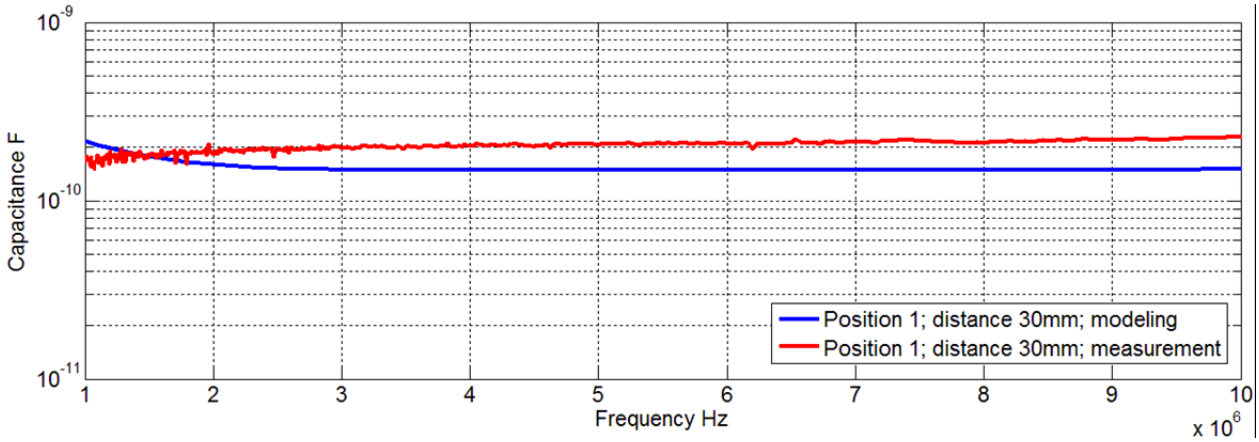


Fig. 6.22. From measurement and modeling results extracted parasitic capacitance; Position 1; 30mm distance

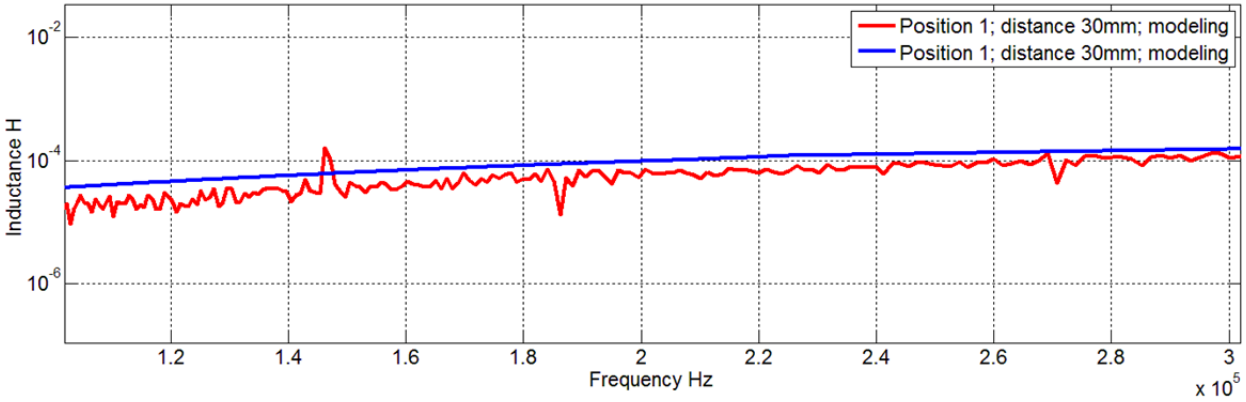


Fig. 6.23. From measurement and modeling results extracted mutual inductance between two inductors; Position 1; 30mm distance

$$L = 2\pi f_1 \left| Z_L(f_1) \right|, \tag{6-1}$$

where

f_1 - frequency in linear region of $|Z_L|$,

$|Z_L(f_1)|$ - impedance at frequency f_1.

Inductive component can also be calculated using Thompson equation as defined in equation (2-78), but it can be also used to verify accuracy of calculated inductive and capacitive components, in case of parallel resonance, calculating resonance frequency. Calculation results are verified using Thompson equation. Resonance frequency is predicted ~1MHz. Therefore, it can be concluded that mutual coupling can be well predicted and analyzed, using CST MSW. In position 1, when inductors are positioned in 30mm distance, extracted mutual inductance is 0.1uH and parasitic capacitance 227pF at 2MHz frequency. Inductance value is slightly changing in frequency range.

All measurement results are analyzed in sense of mutual coupling inductance and parasitic capacitance as in Fig. 6.22. and Fig. 6.23. Modeling results predict measurement results very good. In Fig. 6.24. to Fig. 6.26. mutual inductance and capacitance is presented for all three inductor positions and two inductor distances.

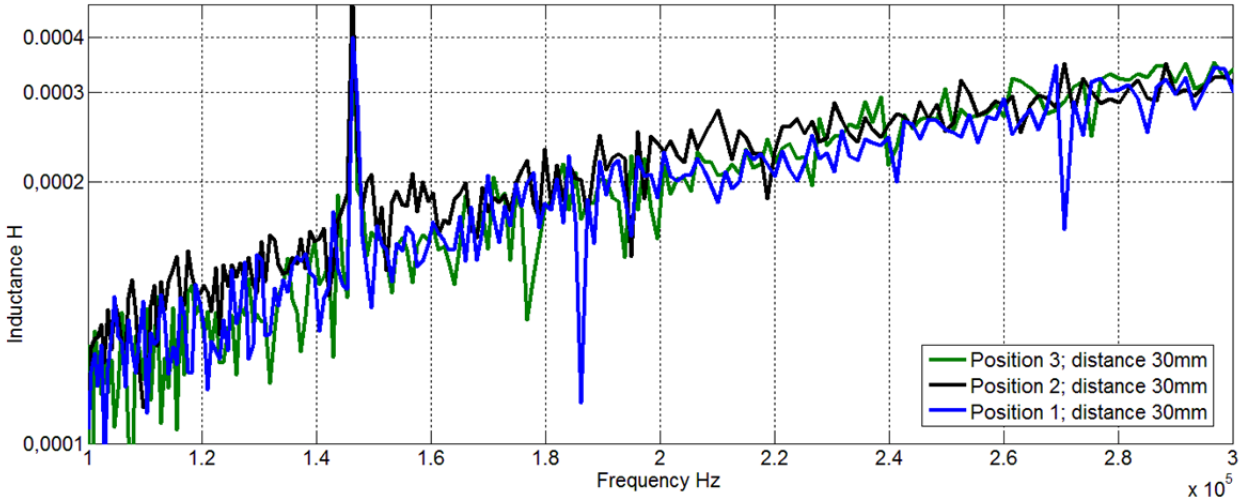


Fig. 6.24. From measurement results extracted mutual inductance between two inductors positioned in 30mm distance

If two inductors are placed in 30mm distance, Position 1 shows the lowest coupling, while Position 2 provides the highest mutual inductance, however difference between extracted results is small. If two inductors are placed in 50mm distance, Position 2 shows the lowest coupling, while Position 3 provides the highest mutual inductance. In contrary to 30mm inductor distance, difference between mutual couplings is reasonable.

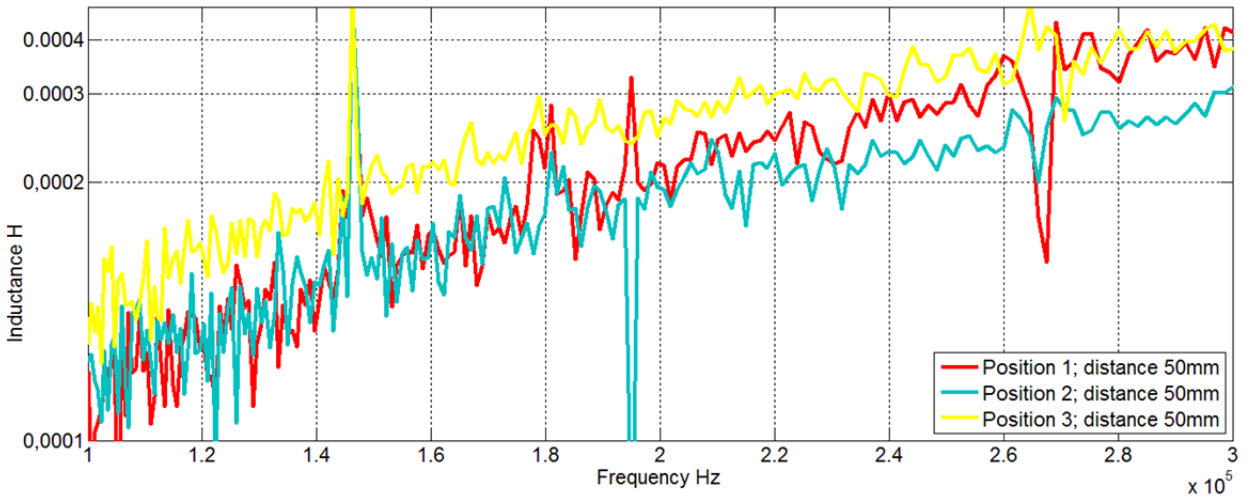


Fig. 6.25. From measurement results extracted mutual inductance between two inductors positioned in 50mm distance

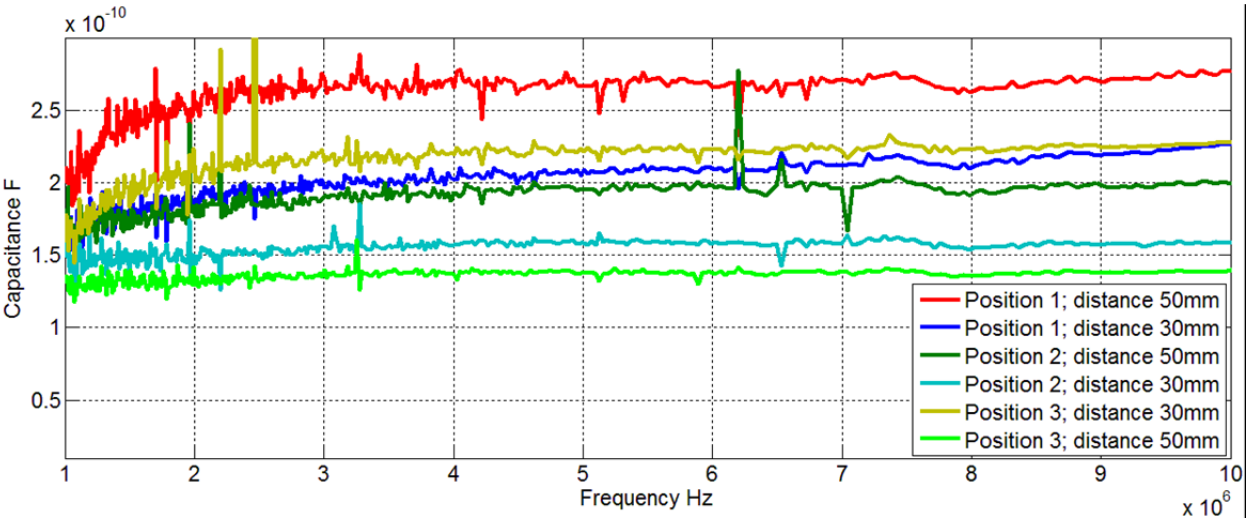


Fig. 6.26. From measurement results extracted parasitic capacitance

Also parasitic capacitance results are inductor position and placement distance dependent, Fig. 6.26. The highest parasitic capacitance is provided by Position 1, when inductors are positioned in 50mm distance. The lowest parasitic capacitance is provided by Position 3 when inductors are placed in 50mm distance. Upper stated measurement results do not give clear answer to the question: “Which position gives the lowest coupling”.

6.5 Mutual coupling reduction between two inductors

It is possible to reduce mutual coupling between two inductors mounted on PCB in close distance using various techniques. One of the possibilities is to use shielding between two inductors and ground plane on PCB. In chapter 5. ground plane and shielding have been analyzed in case if two capacitors are mounted in close proximity. It was discovered that it is very important to connect shielding to ground plane in whole length with low impedance connection. Similar approaches have been used in mutual coupling reduction between to inductors. In this case modeling was used before real prototype measurements, to select efficient shielding design and reduce time for shielding technique development. Afterwards, measurements were carried out to verify applied shielding techniques.

There are three mutual reduction techniques analyzed:

1) application of ground plane (GND);
2) application of ground plane and shielding (shielding is raised 1mm above ground plane and connected in two points to the ground plane);
3) application of ground plane and shielding (shielding is soldered to the ground plane in whole length).

All three shielding technique 3D models are presented in Fig. 6.27. to Fig. 6.29. 3D models are represented as surface current modeling results, to give overview of shielding technique impact on surface currents and close fields. Inductor ferrite cores are not shown in 3D models as surface current is modeled only in conductors.

Initiating left inductor on PCB, it is clearly visible that surface current is present on the ground plane below inductor and in nearby (right) inductor windings, if the shielding is not installed, Fig. 6.27. If shielding is installed and connected in two points to ground plane, surface current is not induced in nearby (right) inductor windings, but surface current is penetrating through slot created by shielding and ground plane- Fig. 6.28. If the shielding is soldered to the ground plane in whole length, the surface current is present only on the excited inductor side (left inductors on PCB)- Fig. 6.29.

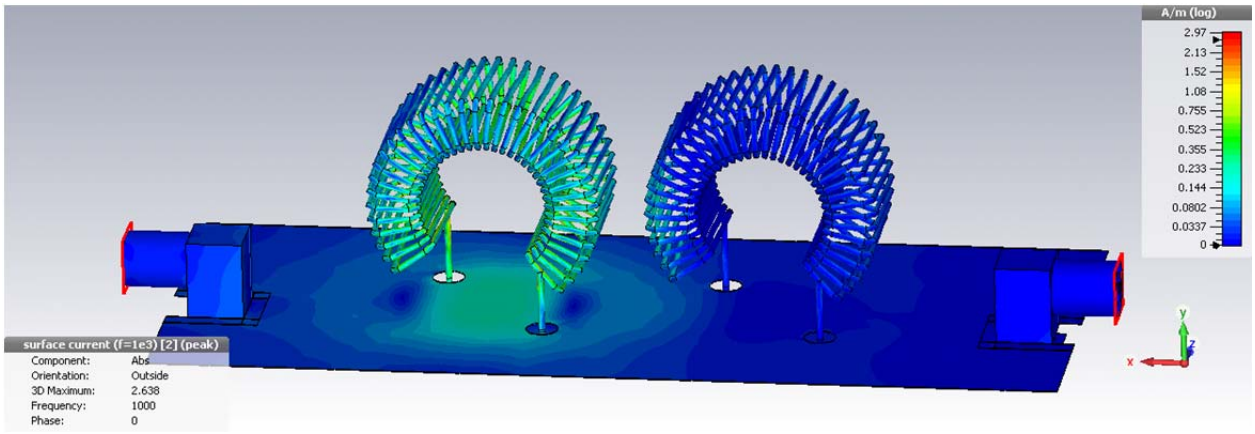


Fig. 6.27. Surface current modeling in CST MSW- mutual coupling reduction using ground plane

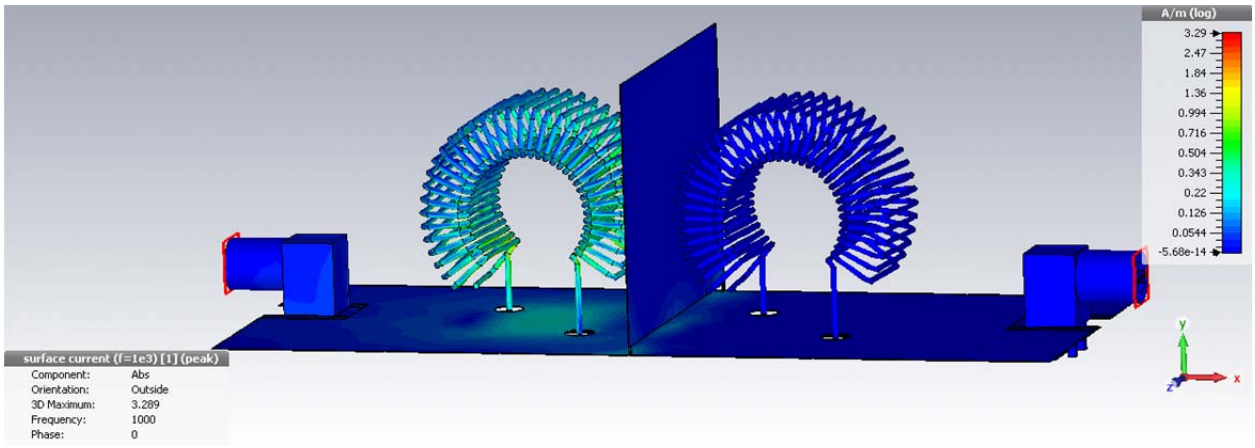


Fig. 6.28. Surface current modeling in CST MSW- mutual coupling reduction using ground plane and shielding connected in two points

Transmission coefficient S_{21} modeling results clearly support surface current modeling results. S_{21} modeling results are presented in Fig. 6.30. Ground plane usage has a little role in mutual coupling cancelation, if shielding is not applied. The shielding between two inductors reduces coupling by at least 10dB and connection style (connection in two points or in whole length) has negligible effect on transfer coefficient. Modeling results predict measurement results very well in whole frequency rage, with static 6dB offset (modeled transfer coefficient is by 6dB higher than measurement results). Up to 1MHz the measured transfer coefficient results are noisy due to the vector network analyzer noise floor.

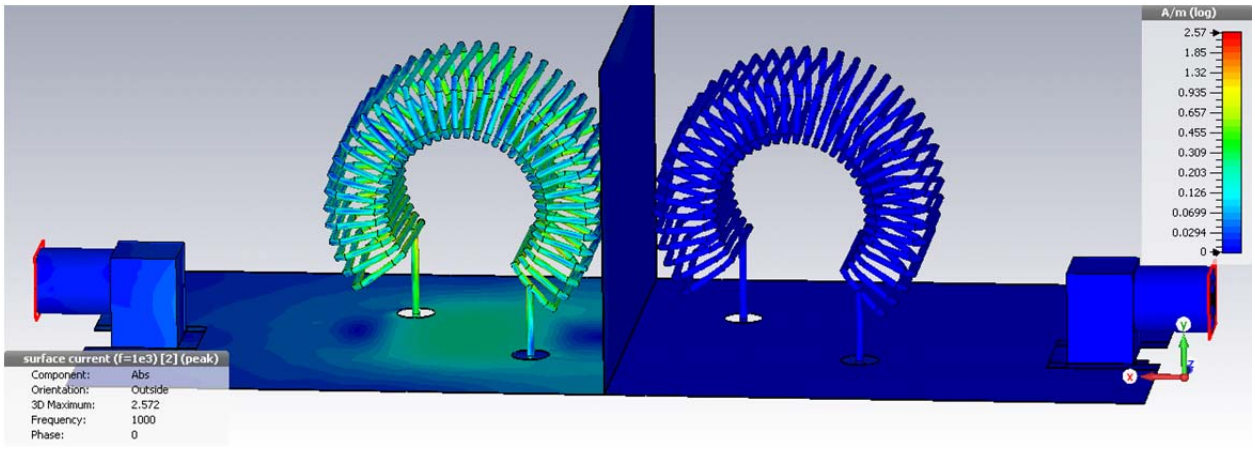


Fig. 6.29. Surface current modeling in CST MSW- mutual coupling reduction using ground plane and shielding soldered in whole length

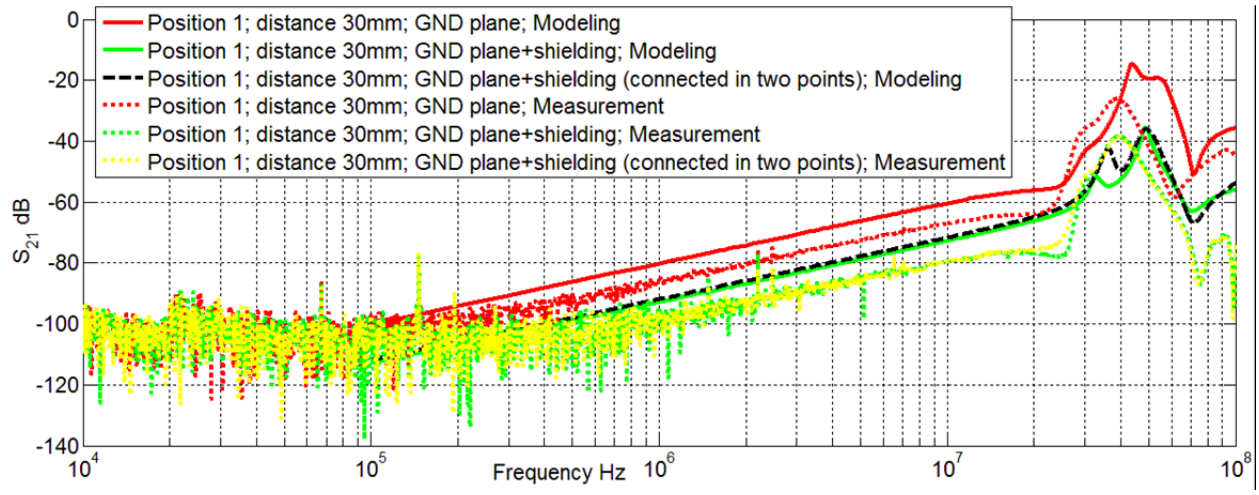


Fig. 6.30. Transfer coefficient S_{21}, modeling and measurement result comparison for different mutual coupling cancelation techniques

Mutual coupling is further analyzed in sense of impedance. If the calculation methodology is used as defined in Chapter 2, exploring measured circuit as two port T-type network and applying equation (2-48). Coupling impedance is calculated in frequency domain, using measurement and modeling results in Fig. 6.31.

In case if only ground plane is used, measurement and modeling results in Fig. 6.30. agree quite well in inductive impedance region- up to 300kHz. In capacitive impedance region- 800kHz to 200MHz, modeling results predict higher impedance than measured one. This can be explained by the fact that modeling predicts lower parasitic capacitance component, Fig. 6.33. Both impedance resonances are predicted with high precision.

In case if shielding is used in addition to ground plane for mutual coupling reduction (connected in two points and connected in whole length), impedance in inductive region is predicted slightly lower than measurement results, due to the fact that predicted mutual inductance is slightly lower than measured mutual inductance- Fig. 6.32. In capacitive impedance region impedance using modeling is not predicted with high accuracy. Predicted parasitic capacitance is lower than measured. Impedance resonance frequencies are predicted quite well.

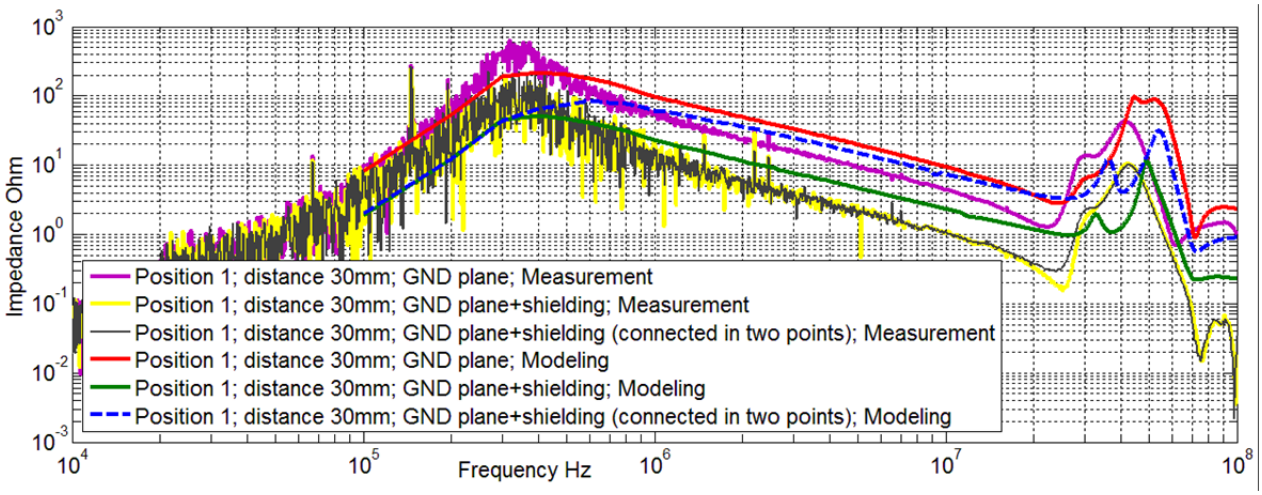


Fig. 6.31. Mutual coupling impedance, extracted from measurement and modeling results

Impedance extracted in Fig. 6.31. can be further analyzed, treating it as parallel LC circuit and extracting capacitive and inductive components that creates first impedance resonance at 350MHz. Further high frequency analysis for ~45MHz resonances is not carried out.

Inductive component can be calculated using impedance that is extracted from S-parameter measured and modeled results. For the calculation equation (6-1) is used. Results are presented in Fig. 6.32. In case if only ground plane is used, measurement results agree with modeling results very well. In case if shielding is used in addition to ground plane, predicted inductance using modeling is slightly lower than measured.

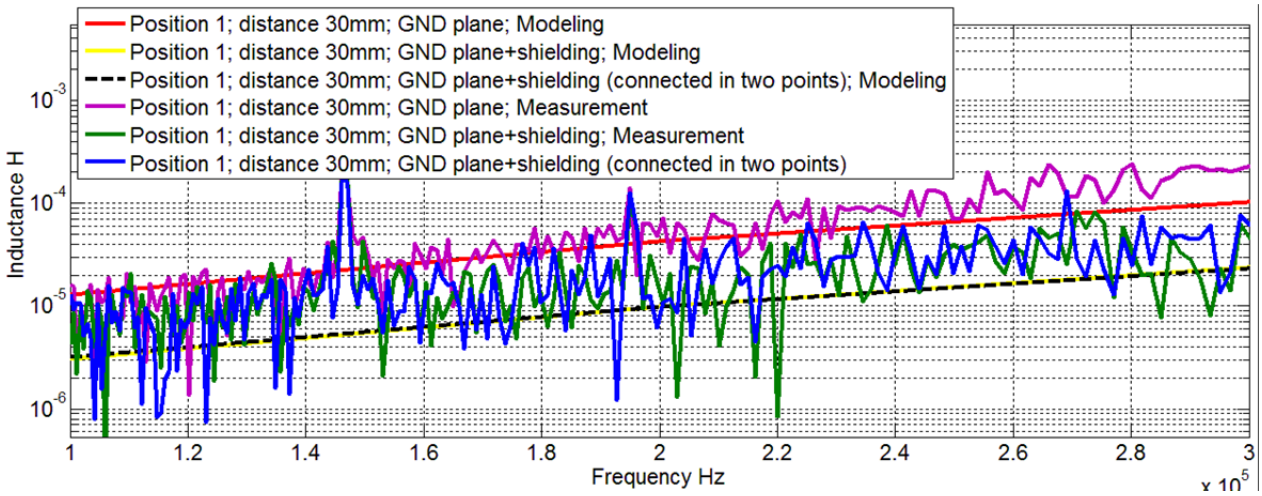


Fig. 6.32. Extracted mutual coupling inductance

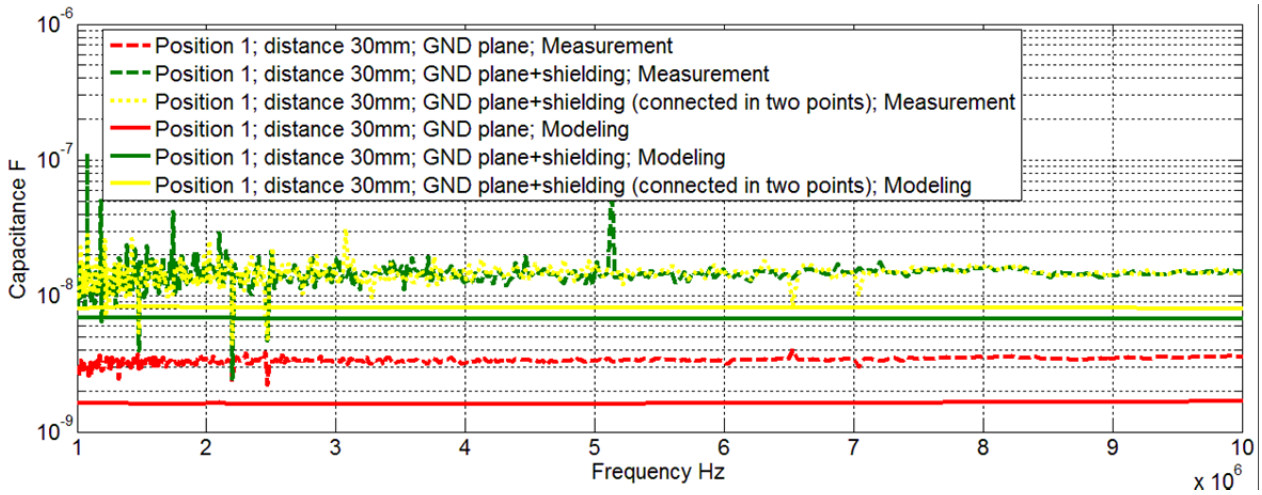


Fig. 6.33. Extracted mutual coupling parasitic capacitance

For capacitive component extraction equation (2-77) is used. Extracted parasitic capacitance results are presented in Fig. 6.33. In all cases modeling results predict slightly lower capacitance than measurement results. In case with ground plane only, parasitic capacitance is lower than in case if shielding is used in addition to the ground plane. Therefore it can be concluded that shielding in addition to ground plane increases capacitive impedance component and decreases inductive impedance component.

6.6 Conclusions

This chapter is devoted to inductor modeling and mutual coupling modeling between two inductors positioned on PCB, using CST MSW. Toroid inductors and PCB boards have been developed to carry out measurements Fig. 6.1.a and Fig. 6.8.a. 3D inductor models have been developed and modeled in CST MWS, Fig. 6.1.b and Fig. 6.8. b. Measurement and modeling results have been compared and they agree very well Fig. 6.13.

The coupling between two inductors positioned on PCB exists. The coupling magnitude is directly proportional to the distance between inductors. Inductor positioning has negligible impact on coupling magnitude, but this conclusion cannot be extended to other situations, as coupling strongly depends on inductor impedance. In cases, if inductor has low inductance, positioning can have considerable impact on coupling.

In addition to conclusions in upper paragraph, this chapter is devoted to CST MSW usage in EMI power filter mutual coupling modeling between two inductors. Filter prototypes were developed and measured Fig. 6.15.a, b, c. Filter 3D models were developed and measured Fig. 6.15. d, e, f. Coupling was analyzed directly in sense of transfer coefficient S_{21} and indirectly extracting coupling impedance. Transfer coefficient results can be predicted with high accuracy using CST MSW modeling- Fig. 6.16. to Fig. 6.18.

CST MSW has been used to predict efficient mutual coupling reduction techniques Fig. 6.27. to Fig. 6.29. Three of them have been modeled and modeling results compared to measurement results Fig. 6.30. Modeling results comply with measurement results with 6dB static (offset) error.

It is possible to successively use CST MSW in EMI power filter inductor impedance analysis, mutual coupling analysis and mutual coupling reduction technique analysis.

7. GENERAL CONCLUSIONS

There is no methodology available for three phase EMI filter component mutual coupling extraction. That could give insight in the importance of proper component selection, placement and routing. There is a couple of papers available regarding conventional EMI filter mutual coupling 3D electromagnetic modeling using dedicated software, but there is lack of information on market driven 3D electromagnetic field modeling software usage in EMI filter modeling. There are lots of researches dedicated to EMI filter component parasitic parameter cancelation, covering analytical aspects mainly. Only few of them cover practical aspects.

In the measurement equipment market dedicated impedance analyzers for high frequencies is a rare and expensive item. For impedance measurement purposes vector network analyzer can be utilized. There is a huge offer in the market with vector network analyzers for lower prices than impedance analyzers. Therefore, scattering parameter usage in EMI filter characterization and filter component characterization methods are developed and measurement errors are analyzed.

The most suitable method for EMI filter capacitor measurement is the reverse transmission coefficient- S_{21}, measurement if two capacitors are connected in parallel with the vector network analyzer ports, as in Fig. 2.9.b. Relative impedance measurement error for this method is below 2.5%, in comparison to other methods that give error up to 250%. The most suitable method for EMI filter inductive component measurements is reverse transmission coefficient- S_{21}, measurement if the inductive component is connected in series with the vector network analyzer ports, Fig. 2.9.c. Relative impedance measurement error for this method is below 1%, in comparison to other methods that give error up to 350%.

Common mode choke alignment (vertical or horizontal) has an influence on following mutual couplings in three phase EMI filter- inductor-capacitor, inductor- input/output trace loops. Mutual inductance between common mode choke and ground plane on PCB reduces the leakage inductance of CM choke. The magnitude of this coupling is affected mainly by CM choke placement above solid ground plane on PCB or other conductive surface in close proximity.

Vertically positioned CM choke above PCB ground plane has larger leakage inductance in comparison to horizontally positioned CM choke when part of the leakage flux is creating eddy current in PCB ground plane. This can be explained by the fact that vertically positioned CM choke has longer connection leads, thus leading to leakage of flux in the air. The magnitude

is affected mainly by CM choke placement above solid ground plane on PCB or other conductive surfaces in close proximity.

Common mode choke alignment (vertical or horizontal) in Π-type filter has an influence on choke related mutual couplings, however impact on filters insertion loss is quite low if comparisons are made with CM choke impact on one phase filters in [41].

Mutual inductance between capacitors in Π-type filter creates shortcut for high frequency disturbance, and dominates over other mutual couplings worsening insertion loss, therefore it should be considered as critical and should be terminated at the first point, when insertion loss improvement of filter should be obtained.

Capacitors can be successfully modeled using 3D electromagnetic software tools available in the market. In this case modeling has been done using CST MWS. Three capacitor models have been proposed. All proposed models during verification have shown that their performance is high enough to enable PCB mounted capacitor modeling and mutual inductance modeling between capacitors. The difference between three proposed capacitor models lays in their complexity that has direct impact on computational time and occupied memory. The first model- Cap1 has the most complex structure having curved faces and round connectors. Therefore, it represents in great details the real capacitor without outer insulation shell. Capacitor models Cap2 and Cap3 are created using rectangular shapes only that leads to lower mesh requirements and lower memory consumption, accordingly. Capacitor model- Cap3 has the lowest meshcell number and the lowest modeling time, whatever solver is used and whatever mesh type is used. In all verification steps all capacitor models have shown that it is possible to model capacitors and their couplings to PCB and other capacitors with great accuracy. Therefore, all capacitor models can be used for this purpose. Therefore capacitor model- Cap3 has at least by 20% lower meshcell number in case if hexahedral mesh type is chosen, compared to capacitor model- Cap2 and at least by 150% lower meshcell number compared to capacitor model Cap1. Capacitor model- Cap3 has at least by 49% lower meshcell number in case if tetrahedral mesh type is chosen, compared to capacitor model- Cap2 and at least by 400% lower meshcell number compared to capacitor model Cap1. Using both solvers and different mesh types it is obvious that Cap3 model calculation takes at least by 30% less than Cap2 calculation and at least by 250% less time than Cap1 calculation, if frequency domain solver with hexahedral mesh is used. For time domain solver the difference in calculation time is higher- Cap3 model calculation takes at least by 16% less than Cap2 calculation and at least by 1280% less time than Cap1model calculation. Capacitor model Cap3 is recommended to use in further EMI filter modeling.

Therefore, it is possible to successively use CST MSW in EMI power filter capacitor impedance analysis, mutual coupling between capacitors and mutual coupling reduction technique analysis.

CST MSW has been used to predict mutual coupling between inductors mounted on PCB and mutual coupling reduction techniques between two inductors mounted on PCB. Measurement and modeling results agree very well. Therefore, it is possible to successively use the CST MSW in EMI power filter inductor impedance analysis, mutual coupling analysis and mutual coupling reduction technique analysis.

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