Quasi-Z-Source Half-Bridge DC-DC Converter for Photovoltaic Applications

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***Abstract*—This paper presents a novel quasi-Z-source half-bridge galvanically isolated DC-DC converter intended for the photovoltaic applications. The topology could be envisioned as an alternative to the boost half-bridge DC-DC converter but the benefit of its symmetric structure reduces the threat of transformer saturation due to the dc flux. The proposed converter features the continuous input current and could be used either with one or two input voltage sources.**

Keywords— impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources

I. Introduction

The impedance-source (IS) galvanically isolated DC-DC converter was proposed in [1] as an alternative power conversion approach for the renewable energy applications, in particular, for PV power systems. In general, the new topology was derived from a classical voltage source full-bridge isolated DC-DC converter by adding a passive IS network (ISN) to its input terminals. The IS network is a two-port passive circuit that consists of capacitors, inductors and diodes in a special configuration. It could be short- or open-circuited without any damages of the main DC-DC converter. Therefore, the IS DC-DC converter combines the basic properties of the voltage source and current source converters, allowing both the buck and boost functions within the single switching stage. Thanks to this unique property, the IS galvanically isolated DC-DC converters are also known as converters for a wide input voltage and load regulation range.

According to the topology of the ISN, the existing IS DC-DC converters could be categorized as Z-Source [1, 2], quasi-Z-Source [3], Trans-Z-Source [4], Trans-quasi-Z-source [4], and Y-source based converters [5]. The quasi-Z-Source (qZS) approach has gained its popularity fast in the renewable energy applications since it features the continuous input current during the shoot-through operation mode and reduced component stresses.

In the switching stage realization, the dominant solution is the full-bridge inverter, which could be realized in a single- or three-phase configuration [3]. The IS DC-DC converter with the push-pull switching stage [6, 7] is characterized with the reduced number of transistors with performance close to the full-bridge counterpart. However, in this topology the transistors must block twice the dc link voltage, therefore their voltage stress is twice higher than in the full-bridge switching stage.

We propose the novel qZS half-bridge galvanically isolated DC-DC converter as an alternative approach to the IS DC-DC converters with a reduced number of switches. In contrast to the push-pull counterpart, it features twice reduced voltage stress of the transistors and a two-winding isolation transformer. The topology is positioned as a power conditioning unit for PV applications with single- or dual-input functionality.

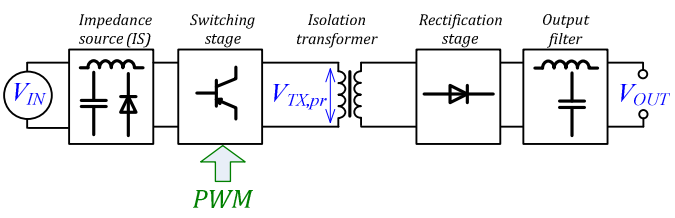


Fig. 1. Generalized block diagram of the impedance source galvanically isolated DC-DC converter.

II. qZS Half-Bridge DC-DC Converter

A. Derivation and general description

Fig. 2 shows the generalized power circuit layout of the proposed qZS half-bridge DC-DC converter. It is based on two identical qZS networks with a neutral node *n* between the capacitors C_1 and C_3. Mirror connection of two qZS networks enables the symmetrical structure of the impedance source network. The topology could be used either with one or two input voltage sources. By help of the voltage doubler rectifier (VDR) the high voltage gain is realized with the optimal turns ratio of the isolation transformer *TX*.

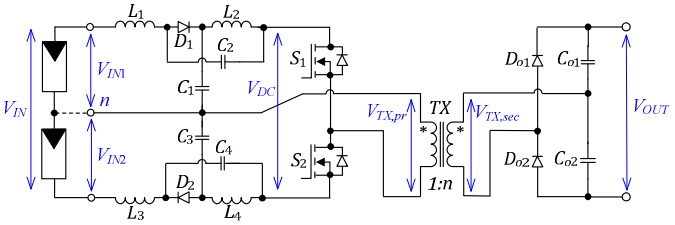


Fig. 2. Power circuit layout of the qZS half-bridge DC-DC converter.

The output voltage of the converter is controlled by the variation of the shoot-through duty cycle of the inverter stage similarly to the qZS full-bridge DC-DC converter discussed in [8]. We examine here the topology with a single input voltage source V_{IN}, therefore the primary winding voltage of the isolation transformer can have three different levels: $-B(V_{IN}/2)$, 0, and $+B(V_{IN}/2)$, where B is the boost factor of the inverter defined as $B=V_{DC}/V_{IN}$.

B. Steady State Analysis

Similarly to any other qZS based galvanically isolated DC-DC converter, the shoot-through states in our topology are generated by the cross-conduction of both switches of the inverter leg (Fig. 3). The switching period in the continuous conduction mode (CCM) consists of two shoot-through states (with a total duration t_S) and two active states (with a total duration t_A), and can be generally expressed as

$$\frac{t_A}{T}+\frac{t_S}{T}=D_A+D_S=1, \qquad (1)$$

where D_A is the duty cycle of the active states, D_S is the duty cycle of the shoot-through states and T is the switching period. The converter is controlled by the symmetrical pulse width modulation (PWM), therefore the active and shoot-through states within one switching period are evenly split into equal intervals of half the duration.

It is seen from Fig. 3 that the proposed topology has three main operating states in the CCM: shoot-through state, positive active state and negative active state.

Shoot-through state [$t_0 < t < t_1$ and $t_2 < t < t_3$]: Shoot-through states are generated by the cross-conduction of S_1 and S_2. The shoot-through state is used to boost the magnetic energy stored in the qZS inductors $L_1...L_4$ without short-circuiting the capacitors $C_1...C_4$. This increase in inductive energy, in turn, provides the boost of voltage seen on the transformer primary winding during the active states of the converter. The equivalent circuit of the converter in this state is presented in Fig. 4*a*. During this state the voltage across the isolation transformer is zero.

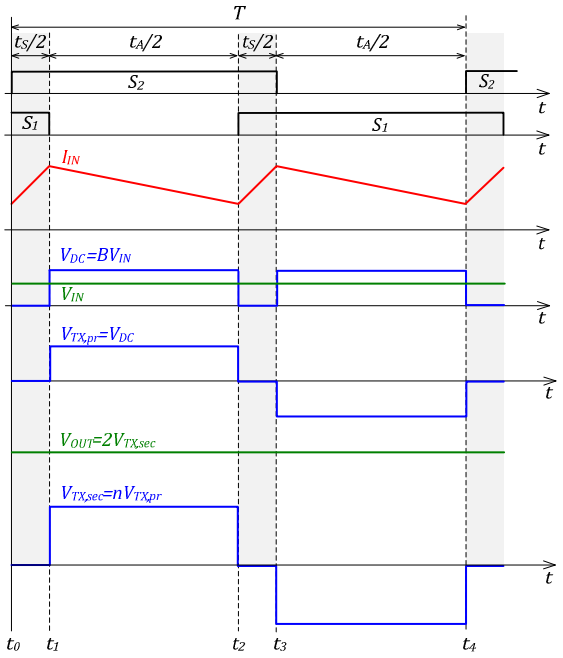


Fig. 3. Control principle and idealized operating waveforms of the proposed topology.

Positive active state [$t_1 < t < t_2$]: During this state, the switch S_2 is conducting, thus resulting in a positive voltage $V_{TX,pr}$ across the primary winding of the isolation transformer. The equivalent circuit of the converter in this state is presented in Fig. 4*b*. It is seen that only the bottom qZS network (C_3-C_4-D_2-L_3-L_4) maintains the power transfer to the output. At the same time, as the inductor L_2 is not involved in the power flow, it charges the capacitor C_2.

Negative active state [$t_3 < t < t_4$]: Switch S_1 is conducting, thus resulting in a negative voltage $V_{TX,pr}$ across the primary winding of the isolation transformer. The equivalent circuit of the converter in this mode presented in Fig. 4*c* is similar to that of the positive active state.

Taking into account that the qZS-network is symmetrical, we can assume that

$$L_1=L_3, \qquad L_2=L_4, \qquad (2)$$

$$C_1=C_3, \qquad C_2=C_4. \qquad (3)$$

Correspondingly, the voltages are

$$v_{L1}=v_{L3}, \qquad v_{L2}=v_{L4}, \qquad (4)$$

$$V_{C1}=V_{C3}, \qquad V_{C2}=V_{C4}. \qquad (5)$$

The sum of the capacitor voltages defines the peak value of the DC-link voltage:

$$V_{DC}=V_{C1}+V_{C2}+V_{C3}+V_{C4}, \qquad (6)$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4} are the average voltages across the capacitors over one switching period. At steady state the average voltage of the inductors over their operating period is zero and the dc voltages of the capacitors can be found from the voltage balance across the inductors:

$$V_{C1}=V_{C3}=\frac{V_{IN}(1-D_S)}{2(1-2\cdot D_S)}, \quad V_{C2}=V_{C4}=\frac{V_{IN}\cdot D_S}{2(1-2D_S)}. \qquad (7)$$

The boost factor of the qZS network can be expressed as follows:

$$B=\frac{V_{DC}}{V_{IN}}=\frac{V_{C1}+V_{C2}+V_{C3}+V_{C4}}{V_{IN}}=\frac{1}{1-2\cdot D_S}. \qquad (8)$$

The gain factor of the proposed converter is expressed as follows:

$$G=\frac{V_{OUT}}{V_{IN}}=\frac{n}{1-2\cdot D_S}, \qquad (9)$$

where n is the turns ratio of the isolation transformer.

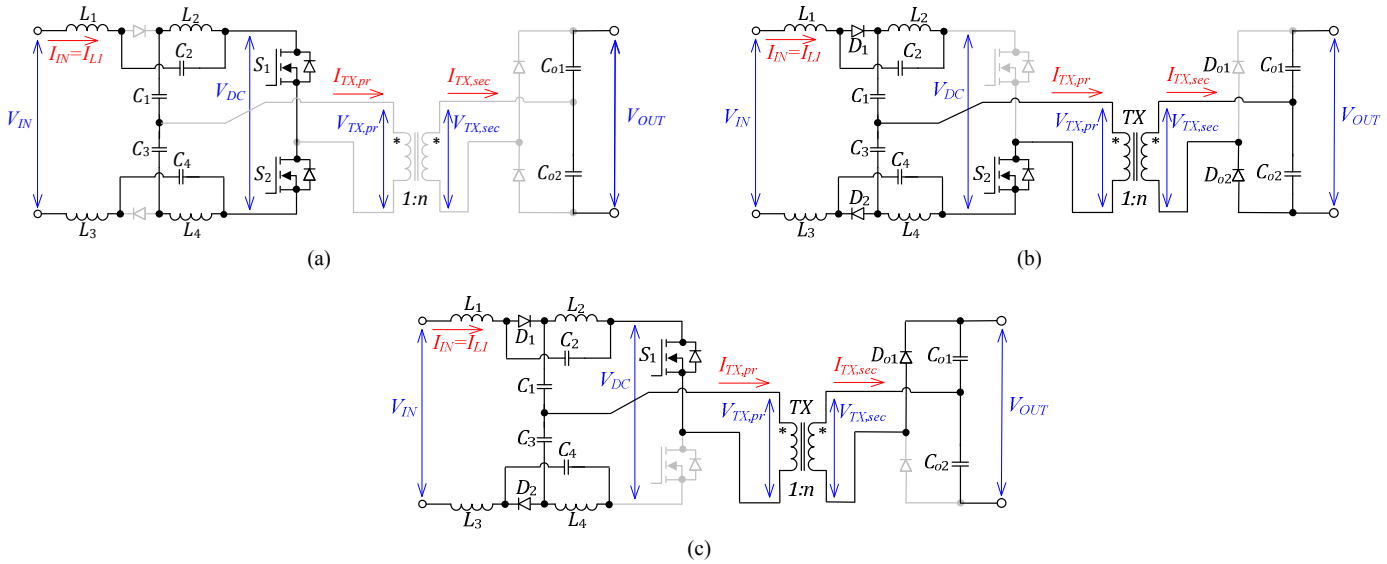


Fig. 4. Equivalent circuits of the proposed topology for its main operation states: shoot-through (a), positive active state (b) and negative active state (c).

C. Component Stresses and General Design Guidelines

The main purpose of the capacitors of the qZS network is to absorb the current ripple and limit the voltage ripple across the inverter. The voltage ripple across the capacitor can be roughly calculated by

$$\Delta V_C = \frac{I_{L,av} \cdot t_S}{2 \cdot C}, \tag{10}$$

where $I_{L,av}$ is the average current through the qZS inductor, C is the capacitance and t_S is the total duration of the shoot-through states over the operating period. In the proposed topology the shoot-through time is evenly split into two intervals of half the duration (Fig. 3) and the qZS network operates with the frequency twice higher than the fundamental frequency of the isolation transformer. Assuming that $C_1 = C_3$ the capacitance needed to limit the peak-to-peak voltage ripple by K_C could be calculated as

$$C_1 = C_3 \geq \frac{P \cdot D_S \cdot (1-2D_{S(\max)})}{f \cdot K_C \cdot V_{IN(\min)}^2 \cdot (1-D_{S(\max)})}, \tag{11}$$

where P is the power rating of the converter, f is the switching frequency, $V_{IN(min)}$ is the minimum value of the input voltage, $D_{S(max)}$ is the shoot-through duty cycle value corresponding to the minimum input voltage, and K_C is the desired peak-to-peak voltage ripple across the capacitor (K_C=$\Delta V_C/V_C$).

Capacitance values for capacitors C_2 and C_4 could be found similarly:

$$C_2 = C_4 \geq \frac{P \cdot (1-2D_{S(\max)})}{f \cdot K_C \cdot V_{IN(\min)}^2}. \tag{12}$$

The inductors in the qZS network will limit the current ripple through the switches during the shoot-through states. Peak-to-peak current ripple through the inductors can be calculated by

$$\Delta I_{L1} = \int_0^{\frac{T \cdot D_S}{2}} \frac{dI_{L1}}{dt} \cdot dt = \int_0^{\frac{T \cdot D_S}{2}} \left(\frac{V_{IN} + V_{C2} + V_{C4}}{2 \cdot L}\right) \cdot dt. \tag{13}$$

The average current through the inductors is equal to the average input current. In order to maintain the CCM operation of the converter, the input current ripple ΔI_{IN} should be smaller than the average input current I_{IN}. Therefore, the minimal inductance value of the qZS inductors where no discontinuous conduction mode (DCM) occurs is

$$L \geq \frac{V_{IN(\min)}^2 \cdot (1-D_{S(\max)}) \cdot D_{S(\max)}}{4 \cdot f \cdot (1-2 \cdot D_{S(\max)}) \cdot K_L \cdot P}, \tag{14}$$

where K_L is the desired peak-to-peak input current ripple of the converter (K_L=$\Delta I_{IN}/I_{IN}$).

To provide correct operation of the voltage doubler rectifier (VDR) and ensure the voltage doubling effect, the capacitors C_{O1} and C_{O2} (Fig. 2) should be properly dimensioned. In order to limit the peak-to-peak voltage ripple on these capacitors by K_{CO}, the capacitance of each capacitor should be

$$C_{01} = C_{02} \geq \frac{P \cdot D_S}{2 \cdot f \cdot K_{CO} \cdot V_{OUT}^2}. \tag{15}$$

The voltage and current stresses on the semiconductors for the ideal system are summarized in Table I.

TABLE I
VOLTAGE AND CURRENT STRESSES OF SEMICONDUCTORS

Component	Maximum Voltage	Average Current
Diodes of the qZS network (D_1, D_2)	$\frac{V_{OUT}}{2 \cdot n}$	$\frac{P}{V_{IN}}$
Transistors of the half-bridge inverter (S_1, S_2)	$\frac{V_{OUT}}{n}$	$\frac{P}{V_{IN}}$
Diodes of the voltage doubler rectifier (D_{O1}, D_{O2})	V_{OUT}	$\frac{P}{V_{OUT}}$

III. Simulation Study

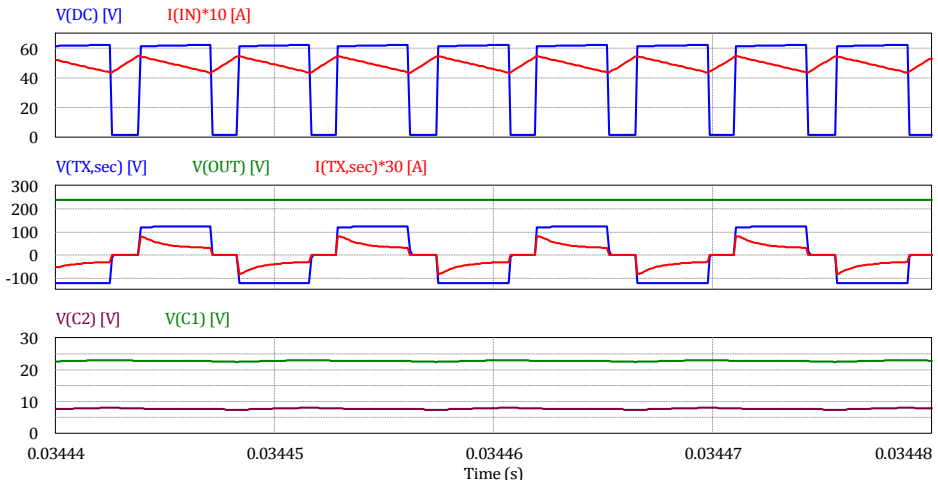
The proposed approach was validated by the computer simulations in the PSIM environment. In the qZS based topologies, the properties of semiconductors have direct impact on the step-up performance of the converter [9], therefore we used accurate models of the semiconductors based on the device datasheet values. To simplify the analysis, the ideal models of passive components (inductors, capacitors and isolation transformer) were used. The simulation parameters and generalized specifications of semiconductors are presented in Tables II and III, respectively. Two operating points corresponding to the maximum and minimum input voltages were studied. In both cases the average input current was kept at its maximum value (5 A). This approach is common for the PV oriented converters, because the PV panel behaves similarly to the current source with the limited output voltage. As shown in Fig. 4, the objects of our study were the input voltage boost properties, input current ripple, quality of the output voltage, and voltage stresses of the qZS capacitors.

TABLE II
Simulation Parameters of the qZS Half-Bridge DC-DC Converter

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	30…58
Maximum input current, A	I_{IN}	5
Output voltage, V	V_{OUT}	240
Switching frequency, kHz	f_{sw}	110
Operating frequency of qZS-network, kHz	f_{qZS}	220 ($2 \cdot f_{sw}$)
Transformer turns ratio	n	4
Capacitance of qZS capacitors, µF	$C_1 \ldots C_4$	26.4
Inductance of qZS inductors, µH	$L_1 \ldots L_4$	24
Capacitance of output capacitors, µF	C_{O1}, C_{O2}	2.2
Converter power rating, W	P	300

TABLE III
General Specifications of Semiconductor Components Used in Simulations and Experiments

Component	Type	Specifications
S_1, S_2	Infineon IPP600N25N3	V_{DS}=250 V; $R_{DS(on)}$=60 mΩ I_D=25 A, Q_g=22 nC, R_g=2.5 Ω
D_1, D_2	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{o1}, D_{o2}	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A



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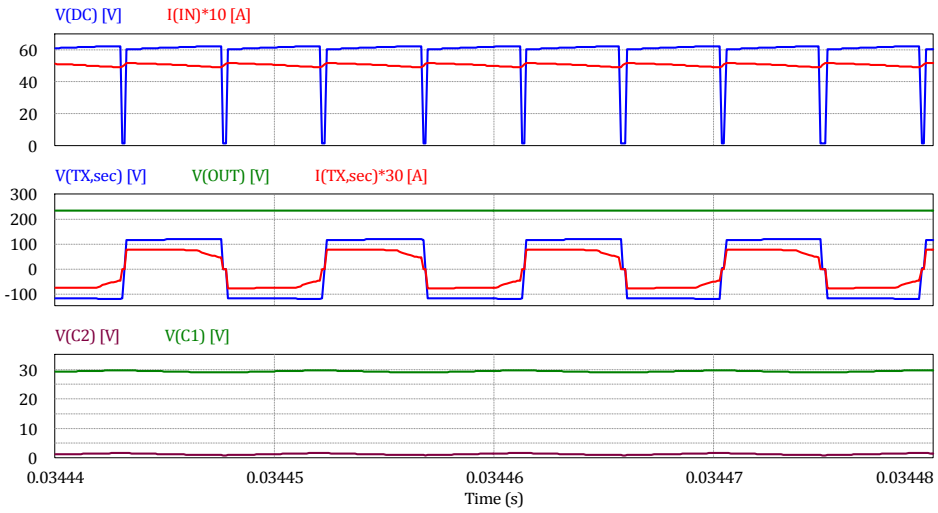

(b)

Fig. 4. Simulation results of the proposed topology at the minimum (a) and maximum (b) input voltages.

In the first operating point with the input voltage of 30 V, the shoot-through duty cycle was set to 0.27 to obtain the desired output voltage. Fig. 4*a* shows that the qZS network ensures the demanded twofold gain of the input voltage (V_{IN} = 30 V and V_{DC} = 60 V) and continuous input current. As predicted by Eq. (6), the amplitude value of the V_{DC} equals the sum of the capacitor voltages of the qZS network. Furthermore, the voltage doubler rectifier provides the demanded voltage doubling effect of the peak voltage of the secondary winding of the isolation transformer, thus ensuring the ripple-free output voltage of 240 V at the power close to 150 W.

Next, the topology was tested with the maximum input voltage (58 V). The shoot-through duty cycle was reduced to 0.05 and the converter operated with the minimal input voltage boost factor (*B* close to 1). As shown in Fig. 4*b*, the operating voltage of the qZS capacitor C_2 (and, consequently, C_4) was decreased almost to zero, while the voltage of C_1 (and C_3) reached its maximum value. It was found that the converter was still maintaining the continuous input current, ensuring the ripple-free output voltage of 240 V at the rated power.

IV. Experimental Results

To verify the proposed topology experimentally, the 300 W prototype converter (Fig. 5) was assembled in accordance with the schematic in Fig. 2 and technical specifications in Table II.

Each qZS network contains the coupled inductor built on the EFD25 core made from N87 ferrite material with the resulting magnetizing inductance of 12 µH. The isolation transformer was wound on the ETD34; its magnetizing inductance was 30.8 µH and leakage inductance referred to the primary was 0.35 µH. Chip monolithic ceramic capacitors SMD1210 2.2 µF 100 V from Murata were used to assemble the qZS network and the voltage doubler rectifier (12 units connected in series for each qZS capacitor and 9 units connected in 3x3 matrix configuration for the VDR capacitors). The types and generalized specifications of the semiconductors are presented in Table III. The prototype was built on the 250 V Si MOSFETs, thus without optimization for the high efficiency.

The experimental setup was supplied from two PV simulators Agilent E4360A connected in series. Each PV simulator produced half of the input voltage of the converter, therefore the string connection of two PV panels was emulated.

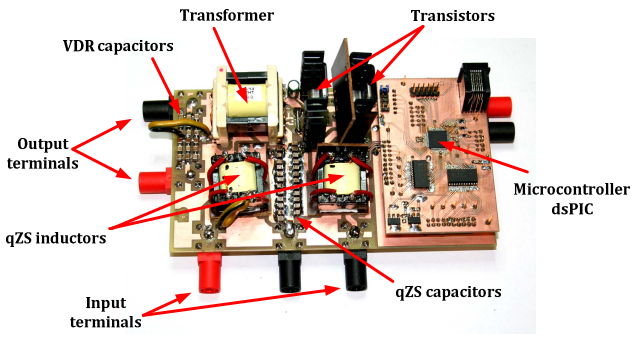

Fig. 5. Experimental prototype (165 mm x 90 mm).

Waveforms measured at the minimum input voltage V_{IN} = 30 V are shown in Fig. 6*a*. Shoot-through duty cycle near 0.3 was used to compensate the losses in the system and to achieve 240 V at the output terminals. Oscillations across transformer windings were observed during the shoot-through states, which is a common behavior of the half-bridge converters caused by the resonance between the transformer leakage inductance and the parasitic capacitance of the semiconductor components [10]. These voltage oscillations are reflected to the qZS diodes D_1 and D_2 that are reverse biased during the shoot-through states.

Waveforms measured at the maximum input voltage V_{IN} = 58 V are shown in Fig. 6*b*. Experimental results obtained somewhat differ from the simulation study (Fig. 4*b*) mainly due to the influence of the leakage inductance of the coupled inductors of the qZS networks and the leakage inductance of the transformer. High number of passive components leads to undesirable oscillations in the qZS network at the operation modes with a DC voltage gain close to unity. For example, these parasitic oscillations have been observed in the input current, as shown in Fig. 6*b*. In both cases the efficiency was limited by 92 %, which is mostly caused by the high on-state resistance of the MOSFETs.

V. Conclusions and Future Work

In this paper the qZS half-bridge DC-DC converter was proposed as a new member of the impedance source galvanically isolated DC-DC converter family. To obtain the symmetrical structure, two identical qZS networks were mirror-connected. Each qZS network needs to handle half of the converter rated power. The topology could be used either with one or two input voltage sources. It has simple control due to reduced switch number and features the continuous input current in the CCM operation.

To validate the proposed topology, the experimental prototype with a rated power of 300 W was assembled and tested. Experimental results have verified all the theoretical assumptions. Voltage stresses of the capacitors and transistors all conformed to the theoretical predictions; however, waveforms of currents were influenced by the parasitic oscillations in the prototype. At the same time, the average values of the currents were not influenced.

Further research will be directed towards the analysis of the resonant processes within the converter and elaboration of the detailed design guidelines. In addition, the operation in the dual input mode with two input voltage sources connected through the common neutral node will be studied.

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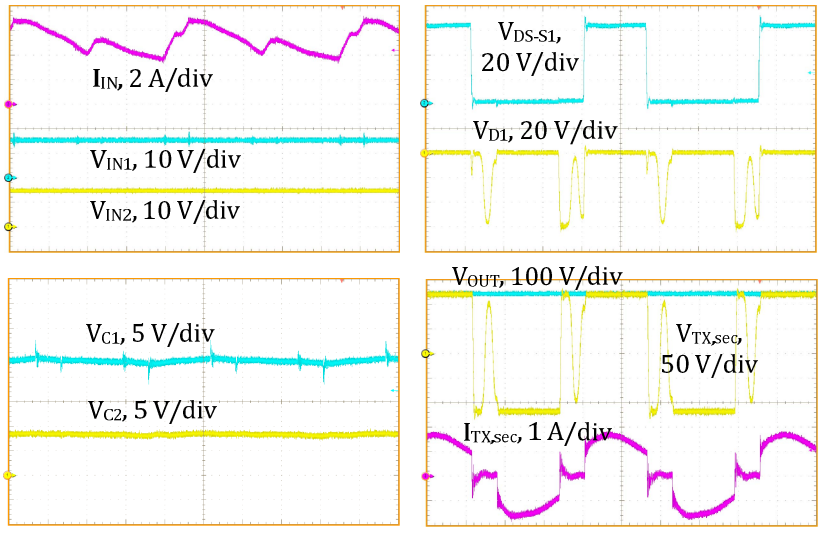

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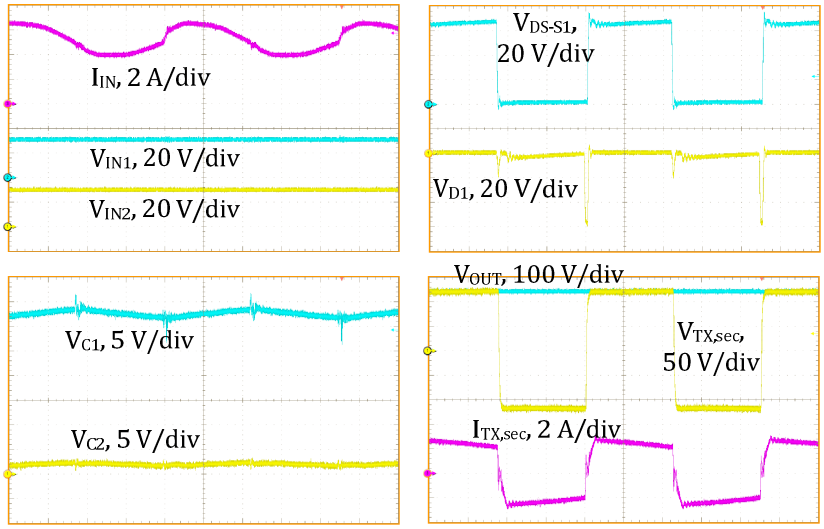

(b)

Fig. 6. Experimental results of the proposed topology at the minimum (a) and maximum (b) input voltages.

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