Analysis of gate drivers for overvoltage suppression in matrix converters for integrated drives

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***Abstract*-This paper describes commutation overvoltage suppression methods by means of gate voltage and current control. Power IGBT gate drive circuits are compared in order to estimate the most compact and efficient topology in terms of gate charge and discharge current. Suggestions for further development of such drivers are made.**

I. INTRODUCTION

There exist a large number of IGBT gate drive circuit topologies and integrated circuits that are used for voltage source inverter arm commutation or in DC-DC converter applications. However commutation of bi-directional switch of matrix converter requires independent gate drive voltage levels for both IGBTs, which means that an independent gate drive circuit for each switching element is required. Moreover the integrated drive concept requires a compact and efficient design of power transistor gate drive circuit, consequently occupying as little space as possible and capable of delivering most gate current.

Power transistors during their turn off undergo overvoltages caused by parasitic commutation loop inductance. These inductances cannot be completely excluded and there is a need in some means of suppression of the overvoltages. Snubber or other clamp circuits may perform this function, but they require additional space and extract some unpredictable heat. This problem may also be solved by a properly designed gate circuit. The same may be done by a well engineered gate drive circuit that slows down the transistor thus keeping the overvoltage smaller. This, however, is done at cost of additional power losses in the transistor itself. At the same time room savings are obvious that is very important for space limited designs like integrated motor drives.

Trade-off between commutation overvoltage and switching times and losses must be found. These technical issues are discussed in the given paper.

II. COMPARISON OF GATE DRIVE CIRCUITS

During this research three most suitable IGBT gate drive totem pole circuits (single-fed half-bridge, full-bridge and double-fed half-bridge) were chosen and experimentally tested. As the power IGBT VT_{IGBT} the IXSN35N120 was used loaded with active load of 600Ω at DC voltage 400V. Square wave generator V_{in} was used to produce control pulses for gate drive circuit with commutation frequency of 20 kHz. Buffer element IC1 ensures sufficient optocoupler IC2 diode current. Optocoupler IC2 provides galvanic separation of control and power circuits. A separated power supply was used to feed the gate drive circuit. The gate current was measured as voltage drop across the gate resistance R_G = 10Ω.

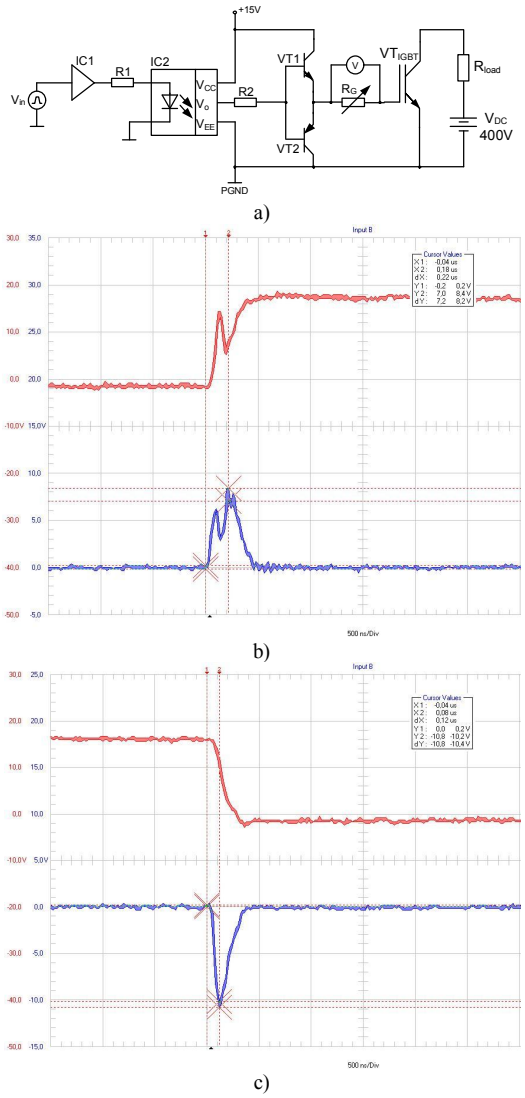
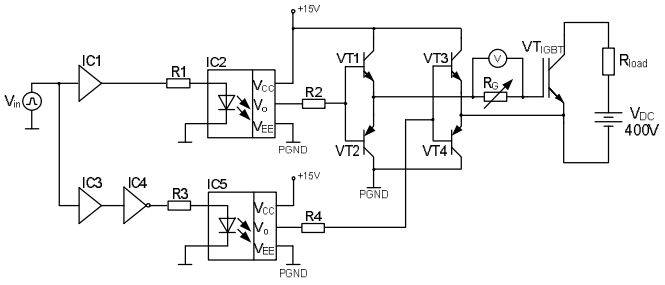


Fig. 1. Single-fed half-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off.



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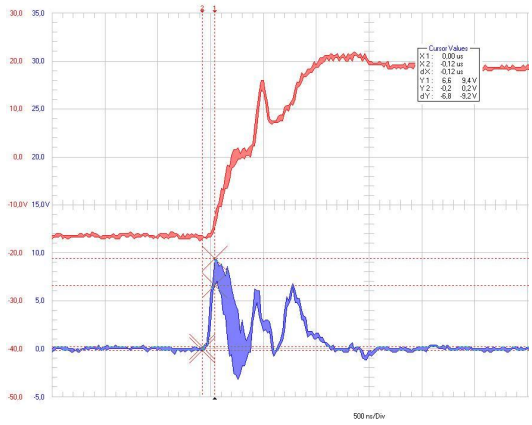

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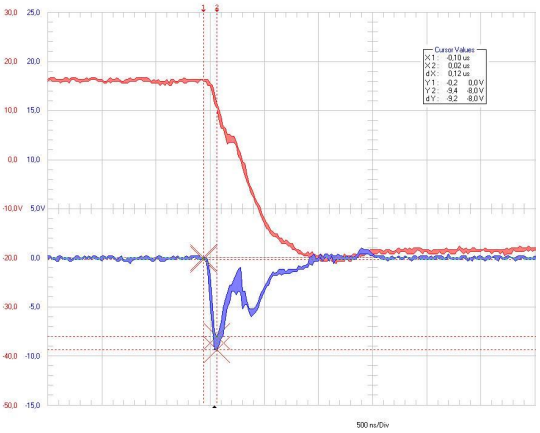

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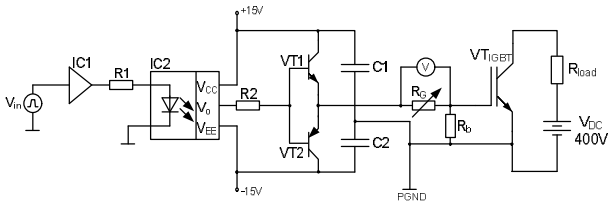
Fig. 2. Full-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off

A. *Single-fed half-bridge circuit*

The simplest circuit of the three mentioned is the single fed half-bridge totem-pole BJT circuit supplied with +15V DC (Fig. 1.a.). This topology consists of two BJTs: high-side transistor VT1 – n-p-n, and low-side transistor VT2 – p-n-p. Since transistors VT1 and VT2 turn on and off inversely, they charge and discharging the power IGBT VT_{IGBT} gate capacitance at the frequency of V_{in}.

When VT1 is on, it applies +15V to gate node of power IGBT. In this case the gate charge peak current $+I_G$ of 0.77A could be achieved. The turn-off of VT_{IGBT} is performed by connecting its gate node to the emitter through VT2 hence applying 0V across the VT_{IGBT} gate-emitter (Fig. 1.b., c.) and a natural turn-off commutation is performed. The discharge current $-I_G$ for this configuration is 1.60A (Fig. 1.c).



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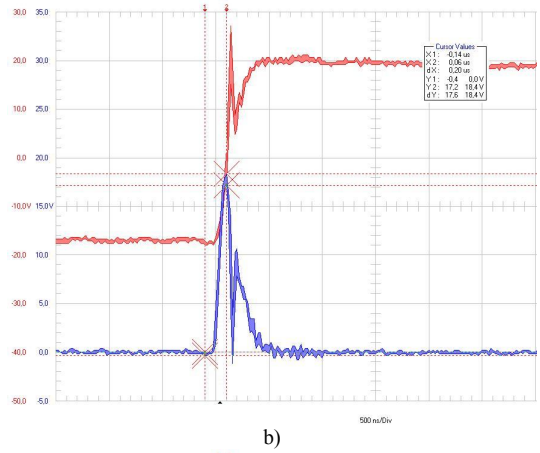

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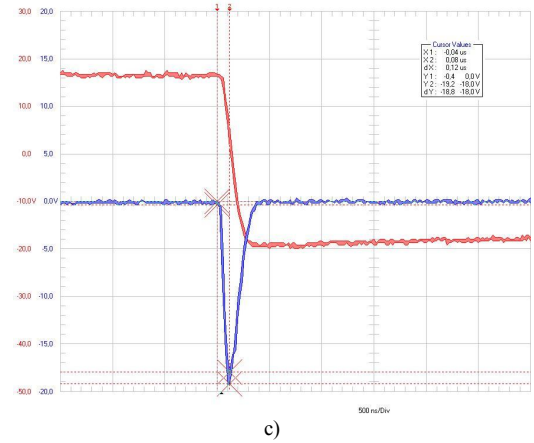

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Fig. 3. Double-fed half-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off.

B. *Full-bridge circuit*

The gate discharge current could be expected higher if forced turn-off commutation is performed. This can be achieved if a full-bridge circuit implemented (Fig. 2.a.). With this configuration +15V and -15V on gate of power transistor can be achieved still using +15V DC supply.

The main drawback of this circuit is the increased number of components. Since one extra totem-pole bridge arm requires another optocoupler IC5 and an inverting circuit IC4. Obviously this configuration occupies more space compared to the previous circuit and is much more expensive.

As can be seen form experimental results (Fig. 2.b., c.) the increase in gate current is not significant. The average gate charge current is 0.80A, and gate discharge current $-I_G$ is even lower than in case of half-bridge configuration, only – 0.86A. Moreover the commutation time has increased due to dead-time that occurs because of switching times of optocouoplers.

C. *Double-fed half-bridge circuit*

As the last the double-fed half-bridge circuit was tested (Fig. 3.a.). Compared to the previous circuit this requires minimum additional elements – only capacitors C1 and C2 and capacitor mid-point balancing resistor R_b. The only drawback of this circuit is the necessity in dual voltage supply that is not always power efficient and space compatible.

Experimental results (Fig. 3.b., c.) show the highest values of gate drive current. At turn-on this circuit is capable to deliver $+I_G = 1.80A$, and at turn-off $-I_G = 1.84A$.

III. OVERVOLTAGE SUPPRESSION WITH GATE DRIVE CIRCUIT

As it was mentioned properly designed gate drive circuit may suppress turn-off transients.

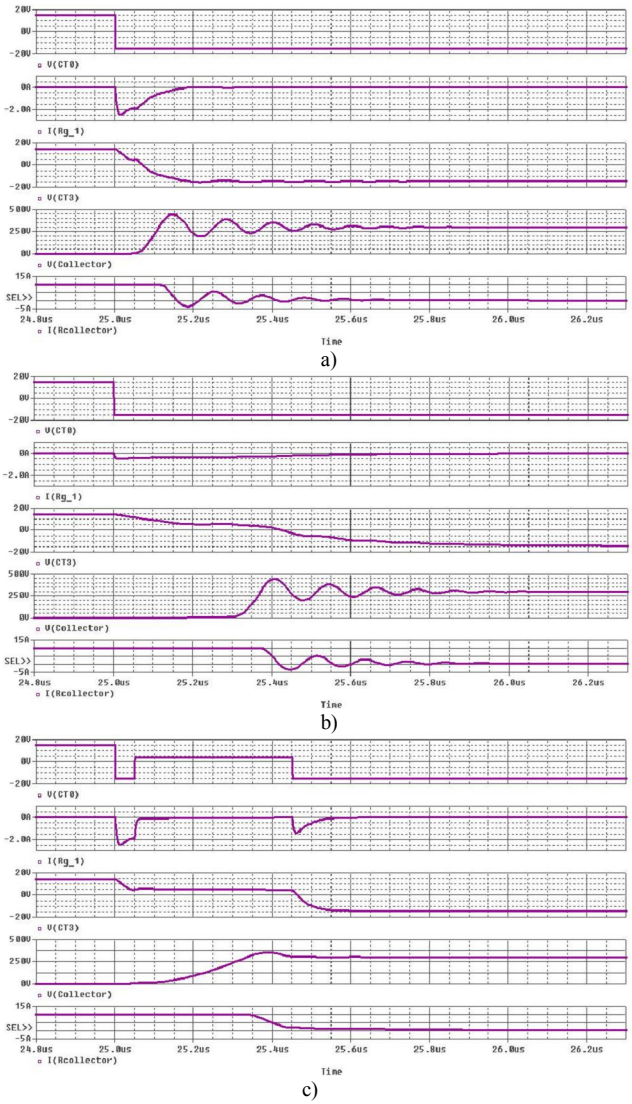

Fig. 4. Voltage controlled commutation transients: a) at R_G=10Ω, b) at R_G=60Ω, c) 2-level voltage controlled turn-off

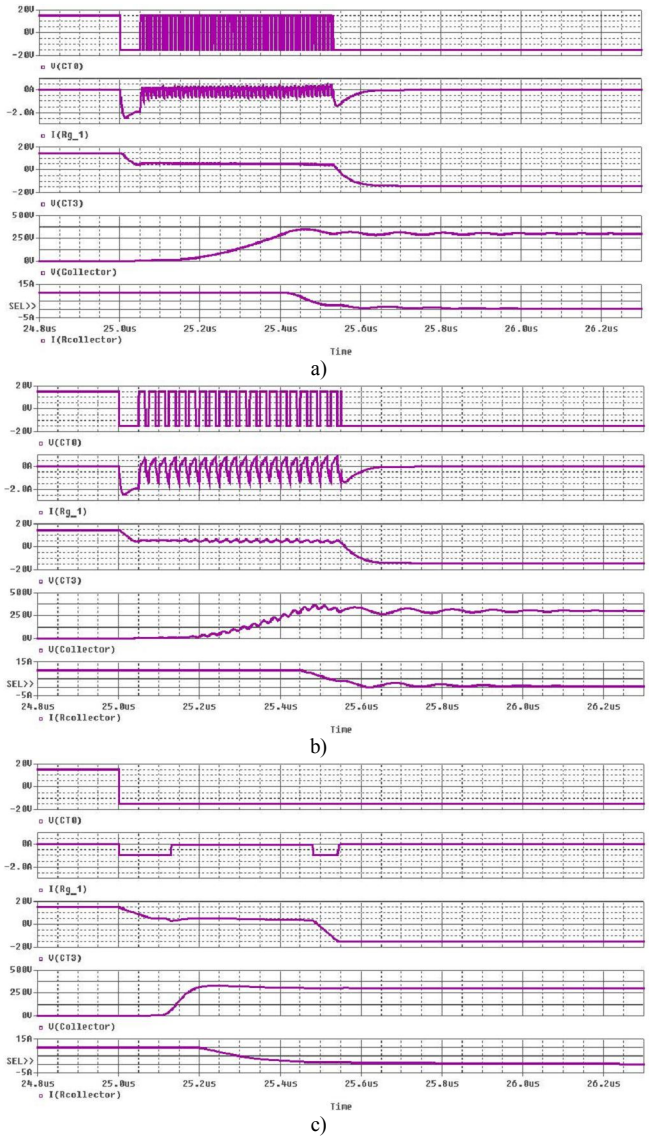

Fig. 5. Turn-off commutation transients: a) voltage controlled PWM at 100MHz, b) voltage controlled PWM at 40MHz, c) current controlled

A. *Voltage controlled turn-off*

The previously chosen half bridge double feed principle is the most compromising solution from the point of view of switching dynamics and space. For particular 300V 10A 20kHz simulation test bench it produces overvoltage of 155V across the power collector-emitter (Fig. 4.a), where from top to bottom: voltage command, gate current, gate voltage, collector voltage and collector current. Here controlling voltage is applied to gate of the power transistor directly through a gate resistor. This fixes gate current of the actual turn-off (voltage rising stage) at the certain level. Smaller negative supply voltage or bigger value of gate resistance will produce just slightly smaller overvoltage of 145V (Fig. 4.b) but at the cost of much slower switching process and, hence much bigger commutation losses.

B. *Two-level voltage controlled turn-off*

Obvious solution – reduction of the applied negative voltage (in fact till the positive values) by means of special circuit only during the most active phase of the switching that takes place at the rising collector voltage and at the falling collector current (Fig 4.c). Reduced negative voltage command (voltage applied to the gate resistor) is activated when the voltage rises above the defined level and removed when the current reaches 0. The command is slightly smaller than the gate voltage corresponding to the load current. The given approach produces 55V overvoltage. There are two significant drawbacks of such solution. First, the voltage reducing circuit itself is very challenging technical task and it is not easy to build such a circuit. Second, reduced voltage varies with the load current that makes the control and measurement more complex. All deviations will lead to re-switching (for higher values) or higher overvoltage (for smaller).

C. *PWM controlled turn-off*

The first problem may be more or less overcome with implementing the PWM principle for reduced negative voltage command (Fig. 5.a). Here, the circuit itself is as simple as the initial one, but speed constraints for its elements are more significant because is a high frequency PWM. Lower frequency of PWM controlled pulses produces significant ripples in the collector voltage (Fig. 5.b). It must also be noted that the second problem – dependence on the load remains.

D. *Current controlled turn-off*

Another way of solving of the mentioned problems is utilizing of a current control principle. Here, the voltage command is applied to the gate through a current regulator. The regulator ensures two levels of the gate current: lower – for the active phase and higher – for the rest of the process (Fig. 5.c). Switching process is not tied anymore to voltage levels and, hence, does not depend on the load. At the same time schematic for current regulators are not very difficult to implement.

E. *Comparison*

Some details of previously shown simulations are compares in Table 1. All mentioned approaches produces smaller overvoltage on the outgoing transistor and all at the cost of the slightly higher power losses. At the same time the PWM approach requires simpler gate circuit, but the current approach – more simple measurement and control for them.

The final conclusion regarding the optimal approach to overvoltage reduction may be done only after experimental investigations that are planned.

TABLE I

COMMUTATION OVERVOLTAGE, TRANSIENT TIME AND COMMUTATION LOSS COMPARISON

Approach	ΔV [V]	ΔT [ns]	ΔP [W]
One level gate voltage @RG=10Ω	155	800	18
One level gate voltage @RG=50Ω	145	1200	20
Two level gate voltage	55	700	26
Gate voltage PWM @100MHz	50	1000	27
Gate voltage PWM @40MHz	60	1300	27
Two level gate current	30	800	25

IV. CONCLUSIONS

It was concluded that the presented experimental data confirms benefits of the half-bridge double-fed totem-pole construction of the gate drivers. It may be used as a basis for more sophisticated control methods like 2-level control strategy. On the other hand, simulation results show that several smart approaches may be implemented. The particular choice is to be made after experimental testing. The final choice will be also dependant on some practical features of implementation like cost and complexity of the design, simplicity of implementation and debugging.

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