INVESTIGATION OF GATE DRIVERS FOR SNUBBERLESS OVERVOLTAGE SUPPRESSION OF POWER IGBTS

Alvis Sokolovs, Iļja Galkins
Riga Technical University, Department of Power and Electrical Engineering
Kronvalda blvd. 1-324, Riga, LV-1010, Latvia
alvis.sokolovs@rtu.lv, gia@avene.eef.rtu.lv

Abstract. This paper describes commutation overvoltage suppression methods by means of gate voltage and current control. Power IGBT gate drive circuits are compared in order to estimate the most compact and efficient topology in terms of gate charge and discharge current. The work is done in context of integrated AC drive with matrix converter. Suggestions for further development of such drivers are made.

Keywords. Overvoltage suppression, active gate driver, IGBT commutation,

1. INTRODUCTION

There exist a large number of IGBT gate drive circuit topologies and integrated circuits that are used for voltage source inverter half-bridge topology commutation or in DC-DC converter applications. However commutation of bi-directional switch of matrix converter requires independent gate drive voltage levels for both IGBTs, which means that an independent gate drive circuit for each switching element is required. Moreover the integrated drive concept requires a compact and efficient design of power transistor gate drive circuit, consequently occupying as little space as possible and capable of delivering most gate current.

Power transistors during their turn-off undergo overvoltages caused by parasitic commutation loop inductance. These inductances cannot be completely excluded and there is a need in some means of suppression of the overvoltages. Snubber or other clamp circuits may perform this function, but they require additional space and extract some unpredictable heat. This problem may also be solved by a properly designed gate circuit. The same may be done by a well engineered gate drive circuit that slows down the transistor thus keeping the overvoltage smaller. This, however, is done at cost of additional power losses in the transistor itself. At the same time room savings are obvious that is very important for space limited designs like integrated motor drives.

Trade-off between commutation overvoltage and switching times and losses must be found. These technical issues are discussed in the given paper.

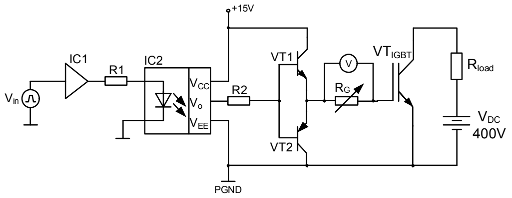
2. COMPARISON OF GATE DRIVE CIRCUITS

During this research three most suitable IGBT gate drive totem-pole circuits (single-fed half-bridge, full-bridge and double-fed half-bridge) were chosen and experimentally tested. As the power IGBT VT_{IGBT} the IXSN35N120 was used loaded with active load of 600Ω at DC voltage 400V. Square wave generator V_{in} was used to produce control pulses for gate drive circuit with commutation frequency of 20 kHz. Optocoupler IC2 provides galvanic separation of control and power circuits. A separated power supply was used to feed the gate drive circuit. The gate current was measured as voltage drop across the gate resistance R_G = 10Ω.

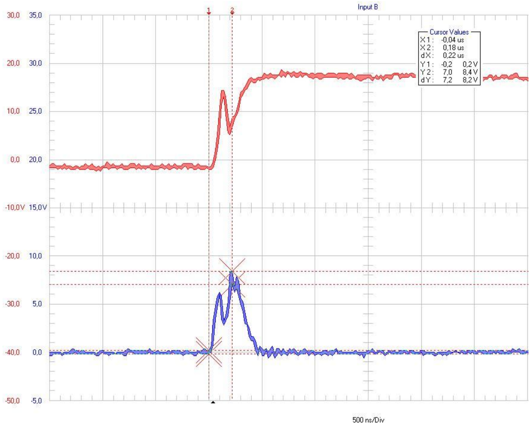
Single-fed half-bridge circuit

The simplest circuit of the three mentioned consists of two BJTs: high-side transistor VT1 – n-p-n, and low-side transistor VT2 – p-n-p (Fig. 1.a.). Since transistors VT1 and VT2 turn on and off inversely, they charge and discharging the power IGBT VT_{IGBT} gate capacitance with the V_{in} frequency.

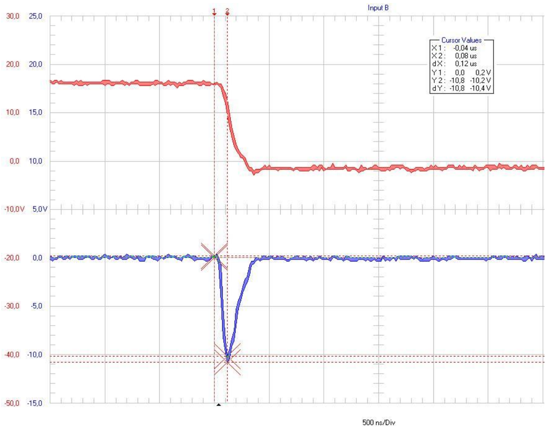
When VT1 is on, it applies +15V to gate node of power IGBT. In this case the gate charge peak current $+I_G$ of 0.77A could be achieved (Fig. 1.b.). The turn-off of VT_{IGBT} is performed by connecting its gate node to the emitter through VT2 hence applying 0V across the VT_{IGBT} gate-emitter and a natural turn-off commutation is performed. The discharge current for this configuration is 1.60A (Fig. 1.c).



a)

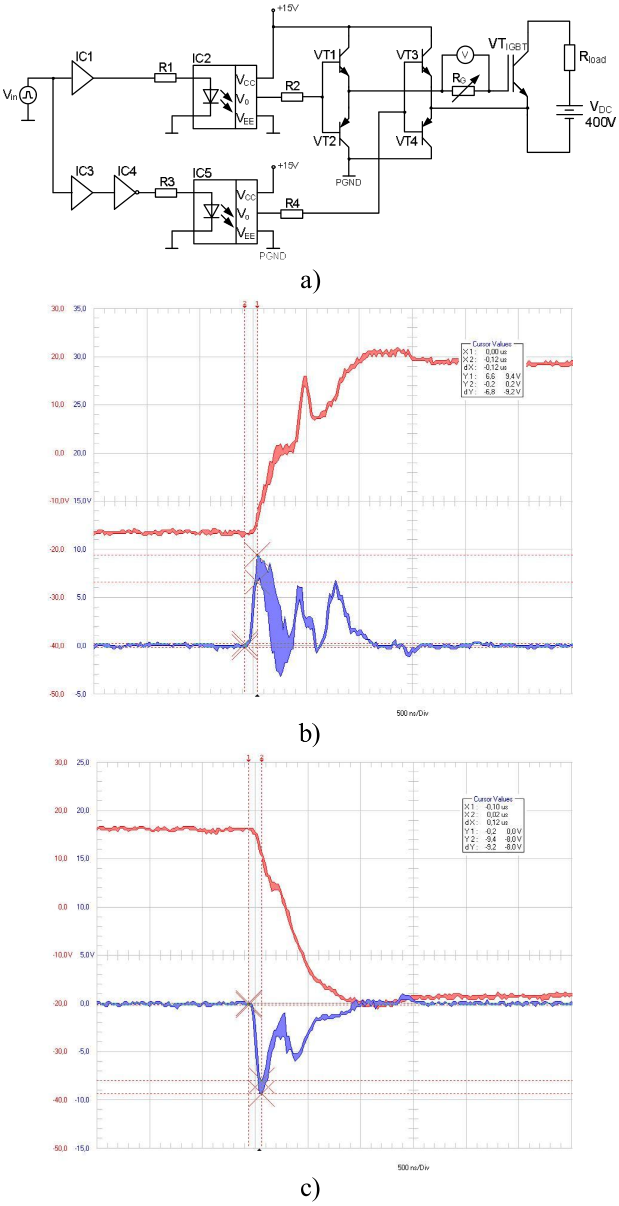


b)



c)

Fig. 1. Single-fed half-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off.



a)

b)

c)

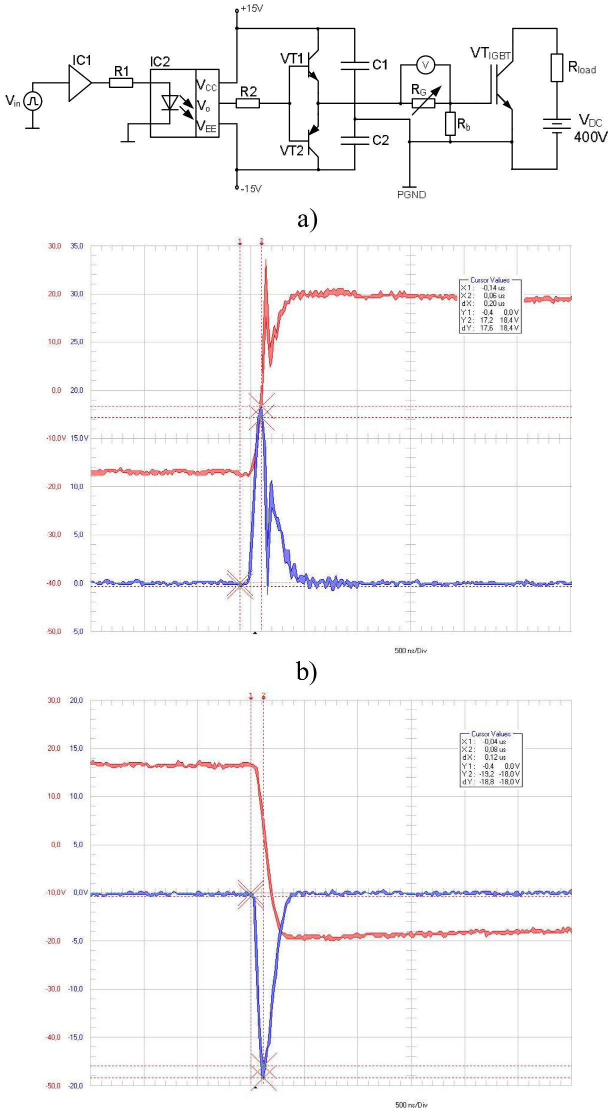
Fig. 2. Full-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off

Full-bridge circuit

The gate discharge current could be expected higher if forced turn-off commutation is performed. This can be achieved if a full-bridge circuit implemented (Fig. 2.a.). With this configuration +15V and -15V on gate of power transistor can be achieved still using +15V DC supply.

The main drawback of this circuit is the increased number of components. Since one extra totem-pole half-bridge, additional optocoupler IC5 and an inverting circuit IC4 is required. Obviously this configuration occupies more space compared to the previous circuit and is more expensive.

As can be seen form experimental results (Fig. 2.b., c.) the increase in gate current is not significant. The average gate charge current is 0.80A, and gate discharge current $-I_G$ is even lower than in case of half-bridge configuration, only – 0.86A. Moreover the commutation time has increased due to dead-time that occurs because of switching times of optocouoplers.



a)

b)

c)

Fig. 3. Double-fed half-bridge totem-pole circuit: a – schematic diagram; b – turn-on; c – turn-off.

Double-fed half-bridge circuit

As the last the double-fed half-bridge circuit was tested (Fig. 3.a.). Compared to the previous circuit this requires minimum additional elements – only capacitors C1 and C2 and capacitor mid-point balancing resistor R_b. The only drawback of this circuit is the necessity in dual voltage supply that is not always power efficient and space compatible. Experimental results (Fig. 3.b., c.) show the highest values of gate drive current. At turn-on this circuit is capable to deliver $+I_G = 1.80A$, and at turn-off $–I_G = 1.84A$.

3. OVERVOLTAGE SUPPRESSION WITH GATE DRIVE CIRCUIT

Voltage controlled turn-off

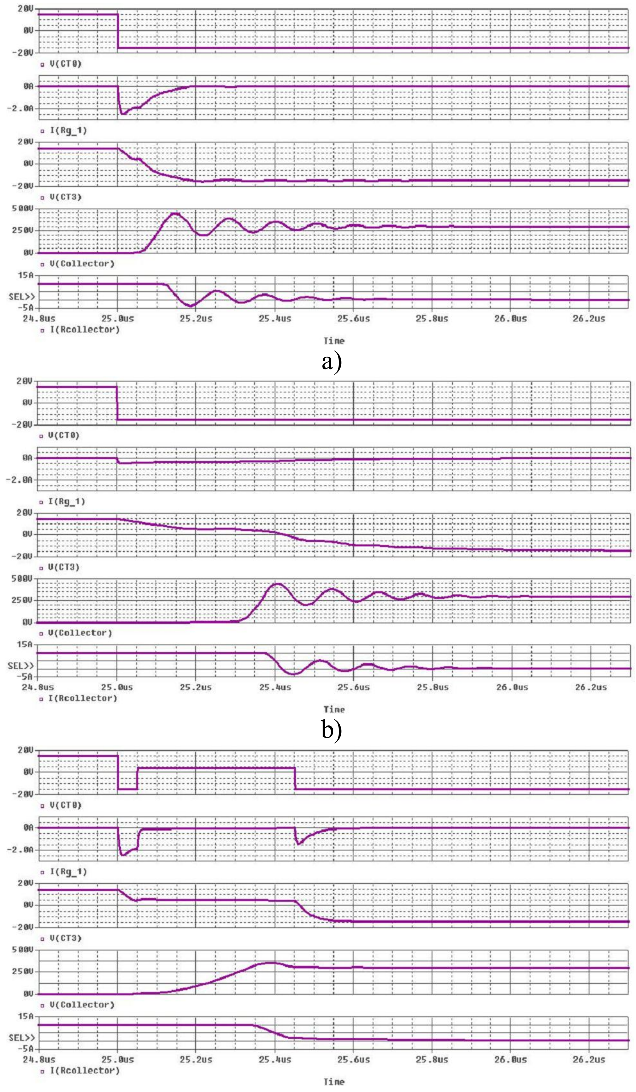
The previously chosen half bridge double feed principle is the most compromising solution from the point of view of switching dynamics and space. For particular 300V 10A 20kHz simulation test bench it produces overvoltage of 155V across the power collector-emitter (Fig. 4.a), where from top to bottom: voltage command, gate current, gate voltage, collector voltage and collector current. Here controlling voltage is applied to gate of the power transistor directly through a gate resistor. This fixes gate current of the actual turn-off (voltage rising stage) at the certain level. Smaller negative supply voltage or bigger value of gate resistance will produce just slightly smaller overvoltage of 145V (Fig. 4.b) but at the cost of much slower switching process and, hence much bigger commutation losses.

Two-level voltage controlled turn-off

Obvious solution – reduction of the applied negative voltage (in fact till the positive values) by means of special circuit only during the most active phase of the switching that takes place at the rising collector voltage and at the falling collector current (Fig 4.c). Reduced negative voltage command (voltage applied to the gate resistor) is activated when the voltage rises above the defined level and removed when the current reaches 0. The command is slightly smaller than the gate voltage corresponding to the load current. The given approach produces 55V overvoltage. There are two significant drawbacks of such solution. First, the voltage reducing circuit itself is very challenging technical task and it is not easy to build such a circuit. Second, reduced voltage varies with the load current that makes the control and measurement more complex. All deviations will lead to re-switching (for higher values) or higher overvoltage (for smaller).

PWM controlled turn-off

The first problem may be more or less overcome with implementing the PWM principle for reduced negative voltage command (Fig. 5.a). Here, the circuit itself is as simple as the initial one, but speed constraints for its elements are more significant because is a high frequency PWM. Lower frequency of PWM controlled pulses produces significant ripples in the collector voltage (Fig. 5.b). It must also be noted that the second problem – dependence on the load remains.



a)

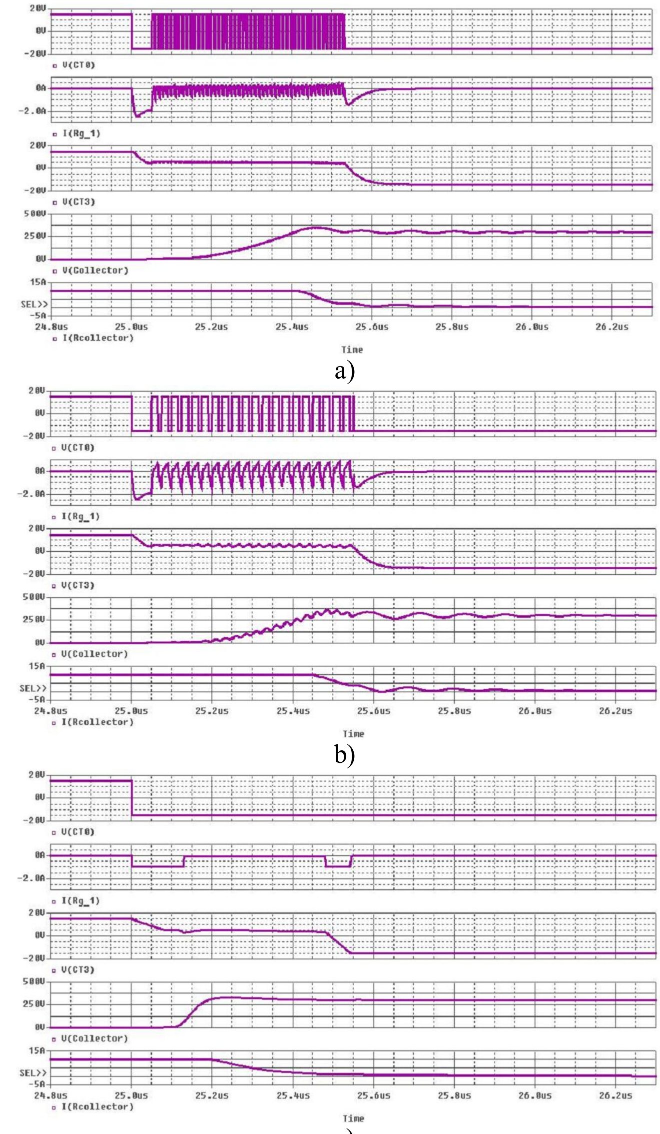
b)

c)

Fig. 4. Voltage controlled commutation transients: a) at RG=10 Ω;.b) at RG=60 Ω, c) 2-level voltage controlled turn-off

Current controlled turn-off

Another way of solving of the mentioned problems is utilizing of a current control principle. Here, the voltage command is applied to the gate through a current regulator. The regulator ensures two levels of the gate current: lower – for the active phase and higher – for the rest of the process (Fig. 5.c). Switching process is not tied anymore to voltage levels and, hence, does not depend on the load. At the same time schematic for current regulators are not very difficult to implement.



a)

b)

c)

Fig. 5. Turn-off commutation transients: a) voltage controlled PWM at 100MHz, b) voltage controlled PWM at 40MHz, c) current controlled

Comparison

Some details of previously shown simulations are compared in Table 1. All mentioned approaches produces smaller overvoltage on the outgoing transistor and all at the cost of the slightly higher power losses. At the same time the PWM approach requires simpler gate circuit, but the current approach – more simple measurement and control for them.

Tab. 1.

Approach	ΔV [V]	ΔT [ns]	ΔP [W]
One level gate voltage @RG=10Ω	155	800	18
One level gate voltage @RG=50Ω	145	1200	20
Two level gate voltage	55	700	26
Gate voltage PWM @100MHz	50	1000	27
Gate voltage PWM @40MHz	60	1300	27
Two level gate current	30	800	25

4. EXPERIMENTS WITH ACTIVE GATE DRIVER

The experiments were carried out on a previously chosen double-fed half-bridge circuit. Since it is necessary to control the value of the turn-off current, the turn-on and turn-off circuit must be split. It can be done by introducing a turn-on diode VD1 in parallel to additional turn-off BJT VT3 (Fig. 5.). When the positive gate voltage is applied to the VTIGBT gate, the VD1 is forward biased and the gate capacitance is charged with maximum current that is determined by RG. The turn-off process, when the negative gate voltage is applied to VTIGBT gate, must be slowed down in order to reduce voltage spikes caused by breaking collector current, as it was simulated and mentioned previously. The turn-off process can be divided into three stages: 1. VT2 and VT3 are open and the gate current starts to increase, hence inducing voltage in the secondary winding of T1, the control circuit reduces conductivity of VT3 hence reducing gate current and slowing down the speed of VTIGBT gate capacitance discharge; 2. the "no-gate current" stage, when the VTIGBT collector-emitter voltage reaches a threshold value, transistor VT3 is closed and gate current is 0; and 3. VT3 is slowly opened, hence ensuring that the negative gate voltage is applied to VTIGBT gate and the transistor is closed.

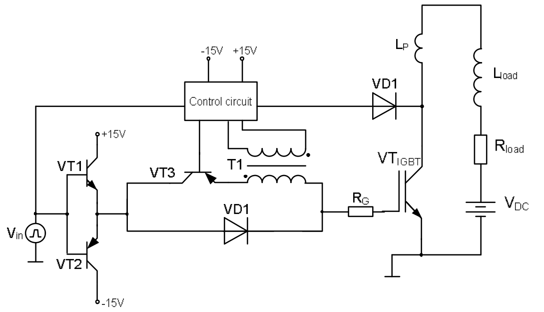


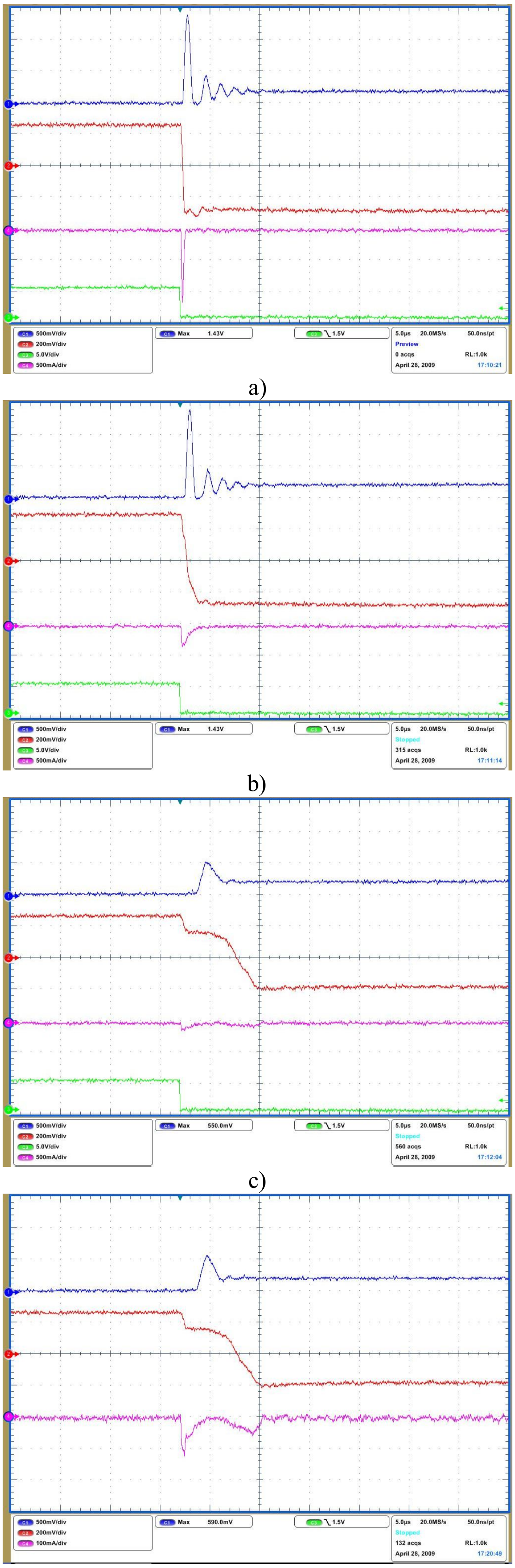
Fig. 5. Experimental setup schematic diagram

Experiments were carried out at supply voltage V_{DC}=100V, load resistance R_{load} = 100Ω, load inductance L_{load} = 56mH and commutation frequency f_c = 5kHz.

The experimental results approve the influence of active gate current control on the reduction of the overvoltage stress of the collector-emitter voltage at active-inductive load commutation.

Experimental results are shown in Fig. 6. (from top to bottom: blue – collector-emitter voltage of VT_{IGBT}; red – gate-emitter voltage of VT_{IGBT}; magenta – gate current of VT_{IGBT}; green – control signal). First experiment was done with RG = 10 Ω, and no active gate current control circuit was involved. As shown in Fig. 6.a. in this case an overvoltage peak of turn-off transient reaches 750V. Second experiment was done with R_G = 68Ω, in order to reduce I_G and slow down commutation of the VT_{IGBT}. As it can be seen in Fig. 6.b. this has little impact on overvoltage, since the active gate discharge in not controlled.

The third experiment involves active gate current control; the results are shown in Fig. 6.c. The commutation time has increased, but the overvoltage spike has reduced to peak value 200V.



d)

Fig. 6. Experimental results of turn-off gate current control a) at $R_G = 10\Omega$; b) at $R_G = 68\Omega$; c) with active gate current control at $R_G = 10\ \Omega$; d) gate current close up

4. CONCLUSIONS

It was concluded that the presented experimental data confirms benefits of the half-bridge double fed totem pole construction of the gate drivers. It may be used as a basis for more sophisticated control methods like 2-level control strategy. On the other hand, simulation results show that several smart approaches may be implemented. Experiments approve effect of gate current control impact on IGBT during turn-off process and it is possible to reduce dangerous collector-emitter overvoltage spikes without use of additional snubber circuits, but it yields more commutation loss inside the transistor. A trade-off between commutation losses and overvoltage suppression must be considered in this case.

More experiments must be done to optimize the first stage of active gate current controlled commutation in order to even more reduce overvoltage spikes and commutation time, which will lead to reduction of commutation losses.

5. REFERENCES

[1] Wheeler, P. W., Clare, J. C., Empringham, L.: “Enhancement of Matrix Converter Waveform Quality Using Minimized Commutation Times”. IEEE transactions on industrial electronics. Vol. 51, 2004. No. 1

[2] Empringham, L., Wheeler, P. W., Clare, J. C.: “Matrix Converter Bi-directional Switch Commutation Using Intelligent Gate Drives”. IEEE 7th International Conference on Power Electronics and Variable Speed Drives. 1998. pp 626 – 631

[3] Ziegler, M., Hofmann, W.: “Semi Natural Two Steps Commutation Strategy for Matrix Converters”. PESC proceedings. 1998

[4] Williams, B. W.: “Power Electronics: Devices, Drivers, Applications, and Passive Components”. 2nd edition. 1992. McGraw Hill. Chapter 3

[5] L. Balogh, “Design and Application Guide for High Speed MOSFET Gate Drive Circuits”, Texas Instruments Application Note

[6] Um, K. J.: “IGBT Basics II”. Fairchild Semiconductor Application Notes 9020. 2002

[7] Mauricie, B., Wuidart, L.: “Drive Circuits for Power MOSFETs and IGBTs”. STMicroelectronics Application notes. 1999. www.st.com

[8] Galkin, I.: “Simple control methods of 3×3 matrix converter”. Scientific Proceedings of Riga Technical University – Section of Power and Electrical Engineering. 2001